



for the PCD1.M0160E0

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0.1 Document History

Version	Changes	Published	Comments
EN01	2013-03-06	2013-03-06	New document
EN02	2013-10-11	2014-02-06	- Logo and company names changed
	2014-01-20	2014-02-06	- Chapter 2.1.1: Instructions for connecting Saia-PCD® controllers to the internet
	2014-01-20	2014-02-06	- Chapter 4.1.1 and 6.1.3: PGND connection on terminal X3 Pin 37
	2014-02-06 2014-04-22	2014-02-06 2014-04-23	- Chapter 4.3: New PCD7.W600 for Slot A - typo corrected
EN03	2014-11-19	2015-03-10	- 5.3 Modbus also for Port #0
	2015-02-10		- Dimensions for screw mounting
	2015-03-10		- Various corrections
ENG04	2016-05-25	2016-05-25	- 3.9 Watchdog Connection example - 4.1.2 Interrupt-Connection - 4.1.4 Digi-I/O-Connection diagram - 4.1.6 Interrupt Device Config - Small fixes
	2018-08-20	2018-08-20	- 4.1.3 wrong text PWM → Digital Outputs

0.2 Trademarks

Saia PCD® is a registered trademark of Saia-Burgess Controls AG.

Technical changes are subject to the state of technology.

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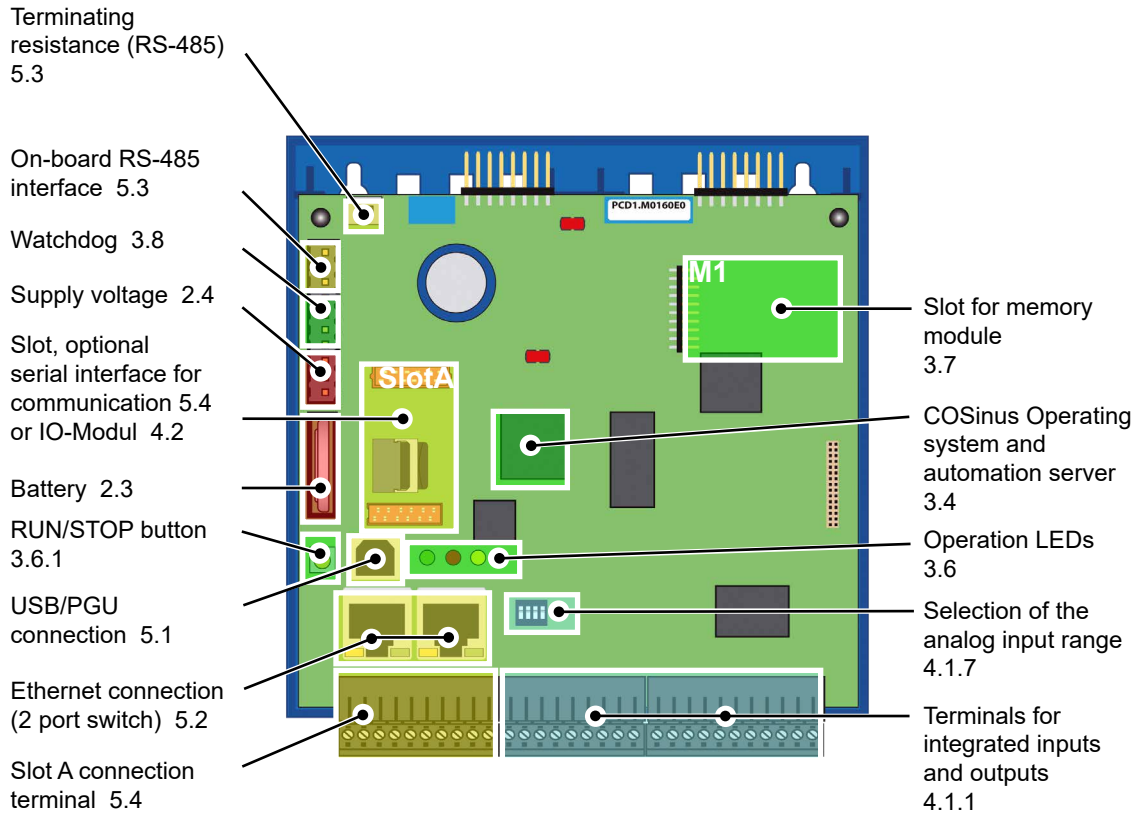
Published in Switzerland

1 Graphical Overview

The graphical overview shows some of the main topics covered in the Operating Manual of the PCD1.M0160E0.



By clicking on the highlighted components and/or connections, you can jump directly to the corresponding chapter in the document.
The numbers separated by dots indicate the relevant chapter numbers.



2 Orientation

Depending on the application, we recommend the following documentation on the topics ...

Topic	Documentnumber, Language, Version and Title
System catalogue	26-215_ENG
Programming tools Saia PG5®	26-732_ENG
Programming	26-733_ENG
Ethernet TCP/IP	26-776_ENG
RS-485 Network	26-740_ENG

2

A wealth of information is available on the support homepage.

Support: www.saia-support.com
 PCD-Homepage: www.saia-pcd.com

2.1 Introduction

This manual describes the technical details of PCD1.M0_ components. Abbreviations (e.g. "LIO") are explained in the annex.

The purpose of this section is to introduce basic principles for the planning and installation of control systems with PCD1.M0_ components.

Details regarding hardware, software, configuration, maintenance and troubleshooting are covered in the respective sections.

2

2.1.1 Instructions for connecting Saia-PCD® controllers to the internet



When Saia PCD controllers are connected directly to the internet, they are also a potential target of cyber attacks. For secure operation, appropriate protective measures must always be taken.

PCD controllers include simple, built-in protection features. However, secure operation on the internet is only ensured if external routers are used with a firewall and encrypted VPN connections.

For more information, please refer to our support site:

www.sbc-support.com/security

2.1.2 Wiring

- The 230 VAC supply cables and signal lines must be routed with at least 10 cm separating them. We also recommend leaving a space between the supply cables and signal lines in the control cabinet.
- Digital signal / bus lines and analogue signal / sensor lines should be routed separately.
- We recommend using shielded cable for analogue signal lines.
- The shielding should be earthed at the inlet and/or outlet of the control cabinet. The shielding should be as short as possible and have the greatest possible cross-section. The central earthing point should be $> 10 \text{ mm}^2$ and be connected to the earthing cable by the shortest route.
- The shielding is normally only connected to the control cabinet on one side, unless the available potential equalisation has a significantly lower resistance than the shielding resistance.
- Inductive loads installed in the control cabinet, e.g. protective coils, must be equipped with suitable suppressors (RC elements).
- Control cabinet components with high field strengths, e.g. transformers or frequency converters, should be shielded by separating plates with a good earthing connection.

Surge protection for large distances or external lines

- With the installation of lines outside of buildings or over large distances, suitable anti-surge measures must be taken. These measures are crucial for bus lines, in particular.
- Lines installed outdoors must have shielding with a suitable power line capacity and be earthed at both ends.
- Surge conductors should be installed at the control cabinet inlet.

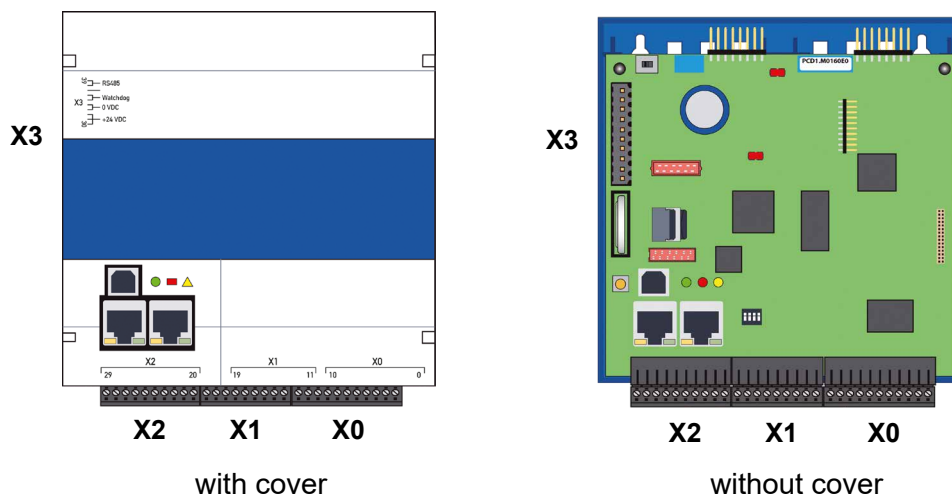
2.1.3 IO Addressing

Optical output position for the following description

The PCD is lying or hanging in front of us as shown, so that the labelling can be read from left to right.

Addressing

Integral I/Os on the CPU board of the PLC are assigned to terminal blocks X0 to X2 and located on the underside of the PLC. They are addressed from right to left, starting at I/O address 32.



All element addresses in the PCD family start from 0

Addressing the inputs or outputs via Saia PG5®



The CPU's on-board inputs and outputs can be assigned to flags and registers (media mapping) by the programmer using the Device Configurator (Device Configurator in the Saia PG5® tool). If IOs are media-mapped, these IOs cannot be reached directly from the program.

Further details about the programming can be found, among other places, in the auxiliary system of the Saia PG5® programming tool or in the corresponding manuals.

Watchdog relay address “O 255”

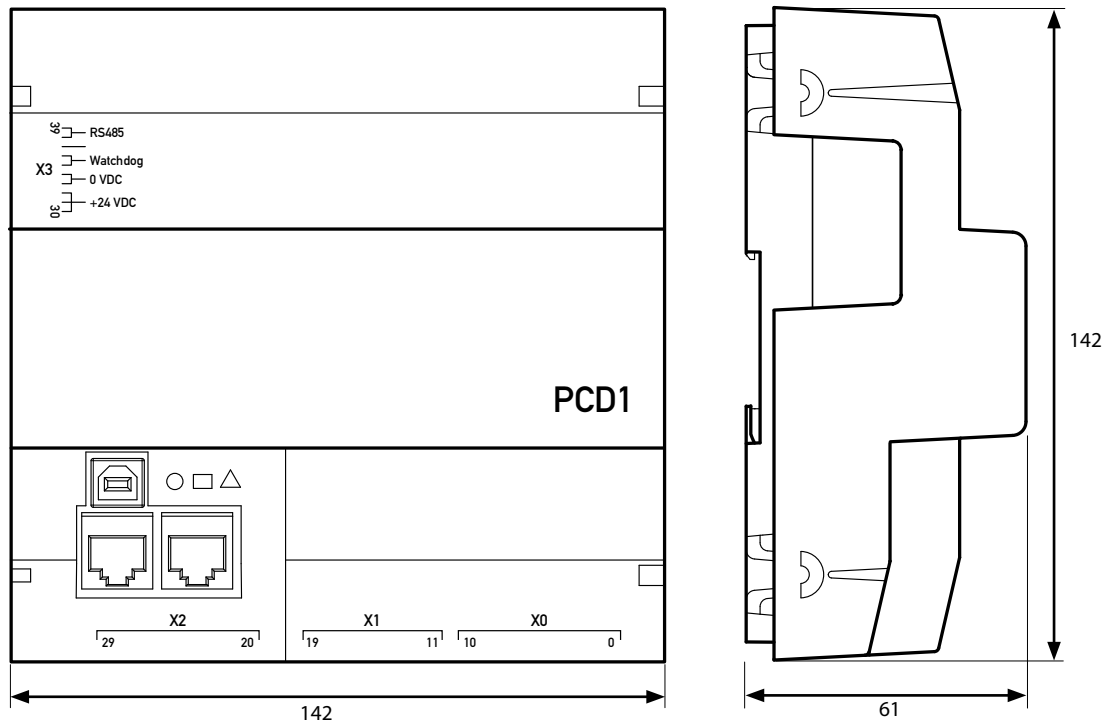
The address O 255 is reserved for the watchdog relay. The closing relay contact connection is located at connector X3.



You can find additional details in Chapter 3.8 Hardware watchdog. Please read this information.

2.2 Installation

2.2.1 Dimensions



Dimensions in mm W x H x D = 142 x 142 x 61

2.2.2 Mounting Position and Ambient Temperature

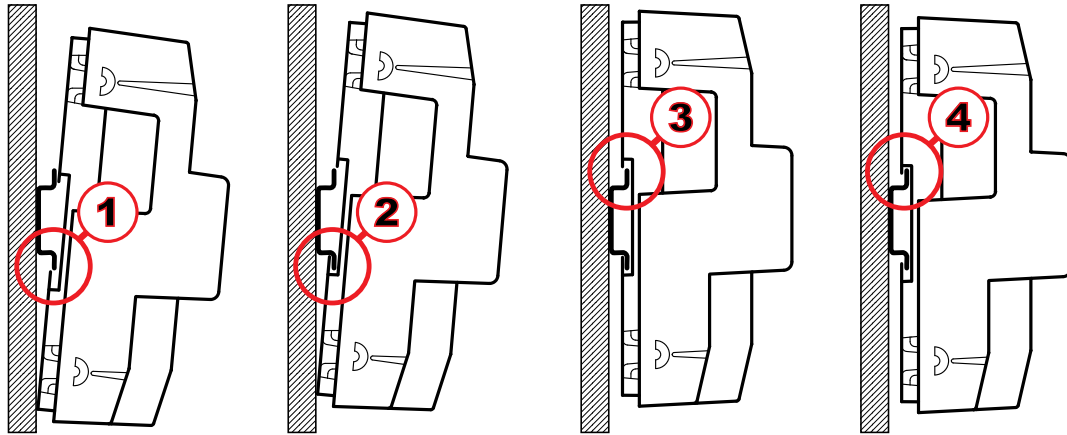
Module holders are normally mounted on a vertical surface, in which case I/O connections to modules are also vertical. With this mounting position, an ambient temperature between 0 °C and 55 °C is permissible.



Vertical mounting should be preferred. All other positions are less favourable to air circulation, so their ambient temperature should not exceed 40°C.

2.2.3 Installation on DIN Rails

The PCD1.M0_ can be snapped onto one horizontally installed top-hat rails (1 x 35 mm according to DIN EN 60715 TH35).



1. Press the underside of the PCD onto the top-hat rail.
2. Slip the lower part of the rail under the two overhanging lugs on the underside of the PCD. Push the PCD upward approx. 1-2 mm. You must overcome the resistance of the four highlighted plastic fingers acting as counter-pressure springs.
3. Press the upper part of the housing against the top-hat rail and snap into the rail, causing the “springs” to give way under the counter-pressure
4. Press the PCD down on the upper edge of the top-hat rail and pull on it gently in order to ensure that the PCD is securely engaged.
5. For removal of the cover, see chapter 2.2.5



Installation Instructions and Recommendations

Installation in Power Distribution Unit

The PCD1.M0160E0 measures 142 × 142 × 61 mm, excluding terminals and connections. For proper installation, a distance of 55 mm above the DIN rail and 75 mm below is recommended.

Ethernet cable

For mounting within the sub-distribution unit, the use of angled or flexible network cable is recommended (e.g. SlimWire PRO). If conventional network cable is installed, it may not be possible to fit a cover onto the sub-distribution unit.

2.2.4 Removal from Top-Hat Rails

The PCD is removed following the above sequence in reverse.

2.2.5 Remove the cover

2

The cover is snapped onto the lower part of the PCD.

PCD1 not yet mounted

1. Hold the PCD1 so that the label reads upside-down. The I/O connections are now at the top.
2. Next rotate the PCD1 until one of its two housing sides is in view.
3. Holding the bottom edge of the housing cover with the fingertips of one hand and the I/O connections in the fingers of the other hand, carefully pull on both parts (housing cover and lower part of PCD1) to separate them.

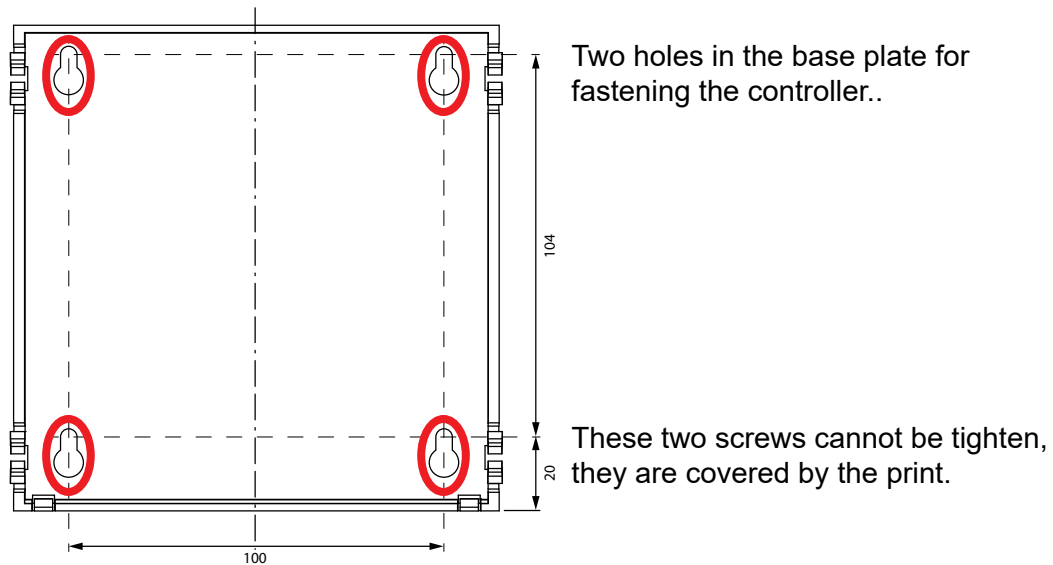
PCD1 is mounted

Pull off the cover with your finger tips beginning from the upper end hooked under the cover edge.

2.2.6 Mounting on a Flat Surface

Mounting on a flat surface is an additional variant using four screws. In the following photograph, the two upper holes are used for fastening the housing and the two lower holes serve as guides.

The following mounting instructions assume that the PCD is to be mounted on a wall in front of the person performing the installation.



1. Remove housing cover as described under 2.2.5.
2. Install all four round-head screws according to mounting dimensions. Screw them down far enough for the PCD to hang on them.
3. Hang the PCD on the four screws.
4. Fully tighten the top two screws. The bottom two screws are provided as guides and are not tightened.

2.3 Battery

Resources (registers, flags, timers, counters, etc.) character strings (TEXT) and data blocks (DBs) are stored in the RAM. In order to prevent these from being lost, and to enable the hardware clock to carry on running during a power failure, PCD1.M0_ devices are equipped with a back-up battery:

2

CPU model	Battery	Buffer time
PCD1.M0_	Renata CR2032 lithium battery	1...3 years ¹⁾

¹⁾ The higher the ambient temperature, the shorter the buffer time

CPUs with lithium batteries are not maintenance-free. The battery voltage is monitored by the CPU. If the battery voltage is $\leq 2,4$ V or the battery is absent, the CPU attempts to start the XOB2. If this is not included in the program, the ERROR LED (yellow) begins to blink with a frequency of 500 ms.

The battery is included and must be fitted during commissioning. For instructions, see chapter 7 Maintenance.

Battery replacement

See chapter 7 Maintenance

2.4 Earthing Concept and Power Supply

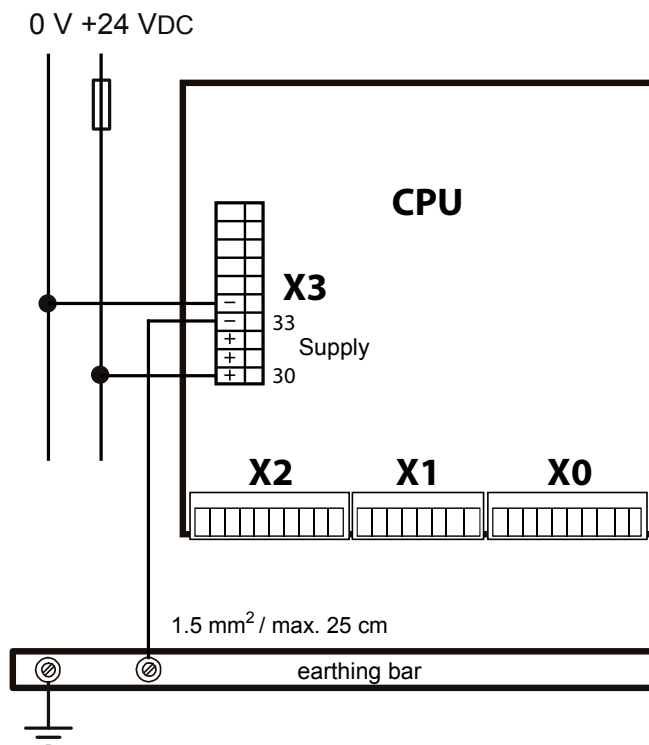
There is a shielding and earthing plate in the lower part of the PCD1.M0_ housing. This combines with the shielding and earthing plate in the module holder to form a common, wide-area earthing point for all I/O modules and the external power supply

2

If an I/O module is inserted in the module holder, the metal claws of the shielding plate in the PCD1 housing form a reliable, multiple contact point with the module.

The zero potential (minus) of the 24 VDC supply is connected to the minus terminal of the supply. This should be connected to the earthing rail using the shortest possible cable (< 25cm) with a cross-section of 1.5 mm².

Any shielding of analogue signals or communications cables should take place either through a minus terminal or through the earthing rail to the same earth potential. All minus connections are linked internally. For problem-free operation, these connections should be externally reinforced with short cables with a cross-section of 1.5 mm².



3 CPU / Processor Unit

3.1 Propertyys of cpu PCD1.M0160E0

Basic unit	PCD1M0160E0
General Features	
I/O bus extension	No
Number of inputs/outputs	18 I/O integrated
Processor	MCF5373L / 234 MHz
Firmware, firmware update (firmware memory soldered on)	Can be downloaded from Saia PG5® environment
Programmable with Saia PG5®	V2.1.030 or higher
RAM expansion	1 MByte
Code/Text/DB	1 MByte (write-protected)
Backup memory	integrated in the file system
User file system	128 MByte
Hardware time precision	Yes, deviation less than 1 min/month
Data backup	Renata CR2032 lithium battery, 1...3 years ¹⁾
Digital inputs	4
Max. Input frequency	1 kHz ²⁾
Digital outputs	max. 10 (1 relay)
Interfaces	
Programming interface	USB ³⁾
Optional serial data interface Port 1 to Slot A	1 × PCD7.F1xxS module RS-232, RS-422/485, MP-Bus or Bluetooth
Port 0 RS-485 (X3 terminal block), up to 115 kbit/s	✓
Profi-S-Net interface/DP slave	Port 0 up to 187.5 kbps
Ether-S-Net interface	2 Port Switch
Field bus connections	
Serial-S-Net	✓
Profi-S-Net/Profibus DP slave	✓

¹⁾ The specified time period is a buffer time, which depends on the ambient temperature (the higher the temperature, the shorter the buffer time)

²⁾ The 1 kHz applies with a pulse/pause ratio of 1:1 and is based on the overall frequency of the inputs.

³⁾ The USB port is type "USB 1.1 Slave Device 12 Mbps" and can only be used for programming and as an S-Bus slave in combination with specific software products (Webconnect, ViSi-PLUS with S-Driver). With a USB 2.0 hub the download takes place twice as fast. It can also be used as a serial data port, for example, in order to connect a terminal; however, this impedes the commissioning and troubleshooting with the Debugger.

3.2 General Technical Details

Power supply (external and internal)	
Supply voltage	24 VDC
Power requirement ¹⁾	typ. 120 mA
Internal bus capacity 5 V / V+	500 mA / 200 mA
¹⁾ In the planning of PCD1 systems, it is especially important to make sure that neither internal supply is overloaded. This check is especially important with the use of analogue modules, counters and positioning modules, because they can have a very high power requirement. For this purpose, we recommend using the specifications in the PG5 Device Generator.	
Ambient conditions	
Ambient temperature	With assembly on a vertical surface with vertically aligned terminals: 0...+55 °C For all other installation positions, a reduced temperature range of: 0...+40 °C applies
Storage temperature	-25...+85 °C
Relative humidity	10...95% without condensation
Vibration resistance	
Vibration	in accordance with EN/IEC61131-2: - 5...13.2 Hz constant amplitude (1.42 mm) - 13.2...150 Hz, constant acceleration (1 g)
Electrical safety	
Protection type	IP20 in accordance with EN60529
Air/leak paths	In accordance with EN61131-2 and EN50178: Between circuits and housings and between electrically isolated circuits: Overvoltage category II, Pollution severity 2
Test voltage	350 V / 50 Hz AC rated unit voltage 24 VDC
Electromagnetic compatibility	
Immunity	According to EN61000-6-2
Electrostatic discharge	According to EN61000-4-2: - 4 kV Contact discharge, - 8 kV Air discharge
Radiofrequency Electromagnetic field Amplitude modulated (radiated)	According to EN61000-4-3: - 2,0...2,7 GHz 1 V/m, - 1,4...2,0 GHz 3 V/m, - 80...1000 MHz 10 V/m
Fast transient burst	According to EN61000-4-4: - 2 kV for direct/alternating current supply lines, - 1 kV for I/O Signal lines and data communication - (2 kV for AC I/O unshielded)
High energy surge	According to EN61000-4-5: - 0.5 kV CM/DM for direct current supply lines, - 2 kV CM and 1 kV DM for alternating current supply lines , - 1 kV CM for I/O Signal lines and data communication - (2 kV CM and 1 kV DM for AC I/O unshielded)
Radiofrequency Interference (conducted)	According to EN61000-4-6: 10 V 150 kHz...80 MHz
Noise emissions	According to EN61000-6-4: for industrial areas

3.3 Hardware version number

After the official release, a product undergoes improvements and modifications in subsequent years. In order to be able to recognise such modifications, there is a so-called hardware version number. Based on this number, the user can check whether a function is provided depending on the hardware. This can be viewed with the Saia PG5® Online Configurator under „Hardware Info“ or on the label on the back side of the PCD1.

3.4 Firmware Version for the PCD1.M0_ (COSinus update)

The firmware of the PCD1.M0_ is stored on a flash memory, which is soldered to the mother board. A firmware update can be applied by downloading a new version with the Saia PG5®. To do so, proceed as follows:

- Open www.sbc-support.com and download the latest firmware version
- Establish a connection between Saia PG5® and the CPU, the same way as when downloading an application (in accordance with the available devices, serial with PGU cable, modem, USB, Ethernet)



A modem connection is never permitted. Modems can block, so that remote access is no longer possible. In these cases, it is necessary to visit the system in person. Other connection options are preferred.

- Open the online configurator and go offline
- In the Tools menu, select “Update Firmware” and use the Browse function to select the path for the file with the new firmware version. Make sure that only one file is selected for download
- Start the download
- After the download, the power supply of the PCD1 may not be interrupted for 2 minutes. (CPLD programming sequence). Otherwise, there is the risk that the CPU locking, in which case it must be sent back to the manufacturer. The download process is concluded with the restarting of the PCD.



The firmware of the PCD1.M0_ is secured on a flash memory on the mother-board.

3.5 System memory structure

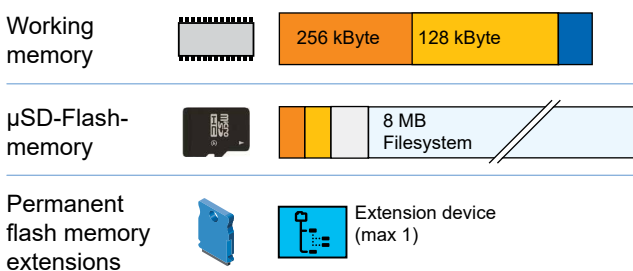
User program code incl. ROM DB/Text	1 MByte saved in the file system
Memory expansion with battery buffer	1 MByte SRAM for read/write access to DB and texts
PCD media with battery buffer	Register: 16'384 Flag: 16'384 Timer/counter: 1600
On-board user file system	128 Mbyte for web files, data logging, documents or backup
PLC file system	Special file system partition PLC_SYS for system data. The user cannot access this partition. This is only for internal use.
Backup for user memory	On filesystem => User BACKUP folder

3.5.1 Memory management of the PCDs with COSinus operating system

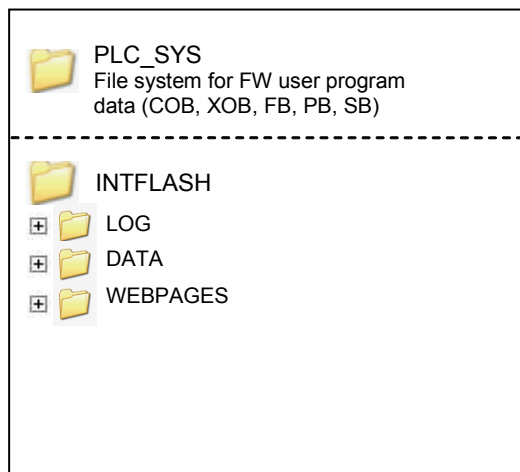
The PCD controllers operate their programs from its internal battery-buffered RAM memory. Controllers such as Saia PCD3.Mxx60, Saia PCD1.M0 _/. M2_ and the programmable Web-Panel MB are equipped with an on-board backup memory (Flash). When downloading an user application with Saia PG5® all necessary files are also stored on request in this backup memory (PG5 default setting).

If the power supply is connected to the controller and there is no executable program in the program memory, during the start-up procedure the PCD (equipped with COSinus OS) is restoring the previously saved program from the backup memory (Flash) into the program memory and then execute it.

Memory structure and resources of the Saia PCD® systems	
Working memory	
User program	256 kByte
DB/Text	128 kByte
Flash memory	
File system	8 MByte (maximum 900 files or 225 directories)
Flash memory extensions	
Extension modules	1



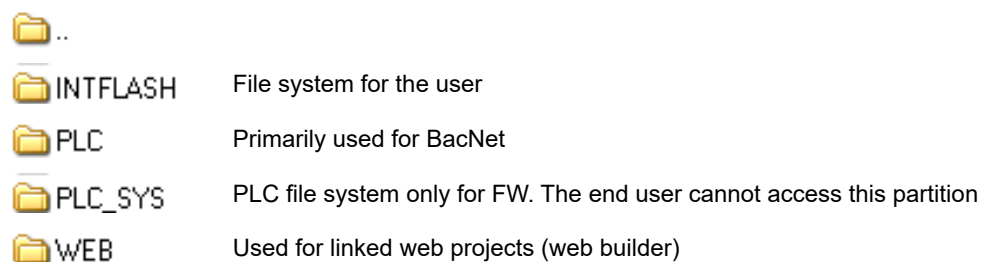
Memory structure of a PCD1.M0160E0 with additional memory cards



Root directory of an SD flash card

3

3.5.2 Flash Memory Structure on PCD1.M0_



3.5.3 On-Board Memory for the File System

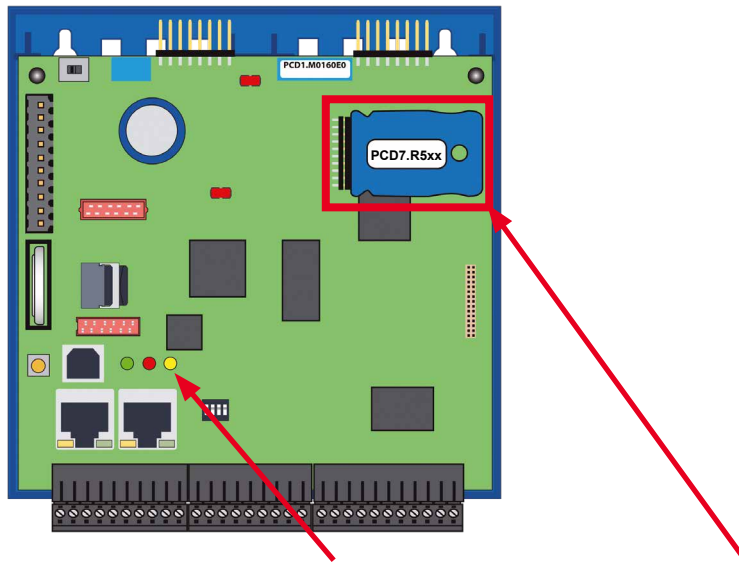
To use the on-board flash memory, select «PCD Memory» → «Internal»



The internal flash memory has the following name:
INTFLASH.

The absolute path for access to the file is as follows:
INTFLASH:/MYFOLDER/MYFILE.TXT






3.5.4 Flash Memory Module PCD7.R5xx for file system



Flash card status LED (yellow) switches on when the permanent flash memory extensions.

The flash card is inserted directly into the main circuit board. A screw in the cover secures the flash card in place. The mechanical cover is designed so that the flash card cannot loosen from the slot due to vibrations.

Memory Modules for PCD1.M0_CPU

	<p>PCD7.R550M04 Flash memory module with file system Enables the saving of files, such as those for the webserver. The PCD can access the files directly through the FTP or HTTP server and write all PC-readable files (*.csv) directly to the module.</p>
	<p>PCD7.R560 BACnet firmware module for slot M1</p>
	<p>PCD7.R562 BACnet firmware module for slot M1 with 128 MB for program storage and file system</p>
	<p>PCD7.R580 Lon over IP firmware module for slot M1</p>
	<p>PCD7.R582* Lon over IP firmware module for slot M1 with 128 MByte for program storage and file system</p>

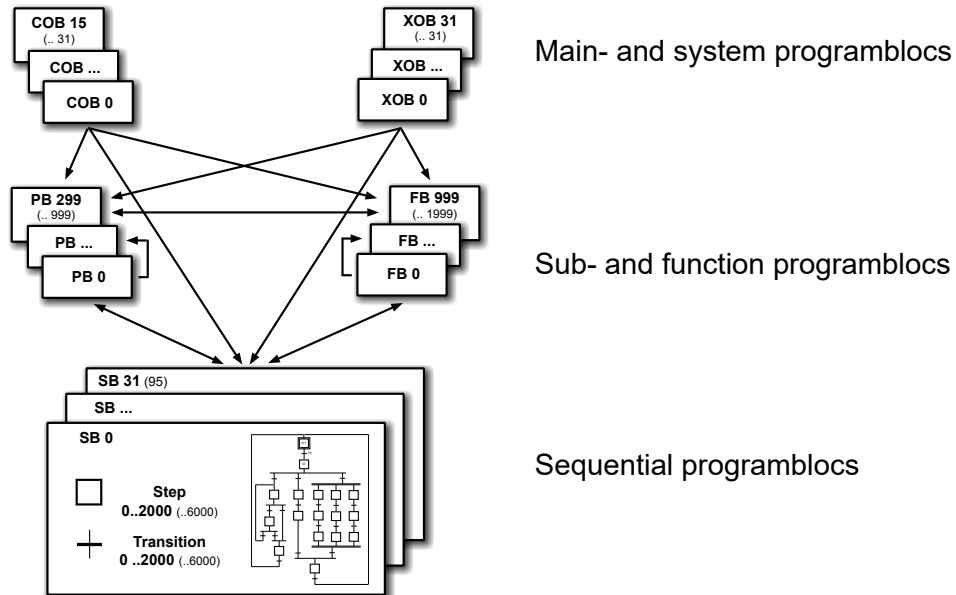
3.6 System resources

3.6.1 Program Blocks

The programmer divides the application program in blocks according to their function.

Model	Number	Addresses	Comments
Cyclical Organisation Blocks (COB)	32	0...31	Main program elements
Exception/system-dependent organisation blocks (XOB)	64	0...63	Called from the system
Program Blocks (PB)	1000	0...999	Subprograms
Function blocks (FB)	2000	0...1999	Subprograms with parameters
Sequential blocks (SB) a total of 6000 steps and transitions	96	0...95	Sequential processes for Graftec programming

Bloc structure



3.6.2 Data Types / Value Ranges

Model		Comments
Integer	– 2'147'483'648 to + 2'147'483'647	Format: Decimal, binary, BCD or hexadecimal
Floating-point numbers	– 9,223'37 × 10 ¹⁸ to – 5,421'01 × 10 ⁻²⁰ + 9,223'37 × 10 ¹⁸ to + 5,421'01 × 10 ⁻²⁰	Instructions for the conversion of values in the Saia PCD® format (Motorola Fast Floating Point, FFTP) to IEEE 754 format and vice versa are provided.
IEEE single precision, IEEE double precision	±1.401 × 10 ⁻⁴⁵ to 3.403 × 10 ³⁸ ±4.941 ⁻³²⁴ to 1.798 × 10 ³⁰⁸	double precision requires two registers (64 bit)

3

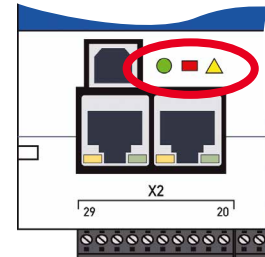
3.6.3 Resources elements

Model	Number	Addresses	Comments
Flags (1 bit)	16'384	F 0...16'383	Flags are not transient, but a transient range, starting from Address 0 can be configured.
Register (32 bit)	16'384	R 0...16'383	For integer or floating point values
Text/data blocks	8191	X or DB 0...8190	For text and DB
Timer/counter (31 bit)	1600 ¹⁾	T/C 0...1599	The breakdown of timers and counters can be configured. Timers count down periodically under the control of the operating system; the basic time unit can be varied between 10 ms and 10 sec- onds.
Constants with media code K	user-defined	0...16'383	Values can be used in instructions instead of registers
Constants without media code	user-defined	-2'147'483'648 to +2'147'483'647	Can only be loaded to a register with an LD command and cannot be used in instructions instead of registers.

¹⁾ To avoid unnecessary load on the CPU, no more timers should be configured than required.

3.7 LED behavior

Three LEDs (green, red and yellow) show the possible operating statuses of the CPU as set out in the following table.



3

LED	PCD1.M2_		
Meaning	Run	Stop	Error(s)
Form	●	■	▲
Colour	green	red	yellow
Run	●	□	▲
Run conditional	●/○	□	▲
Run with error	●	□	▲
Run conditional with errors	●/○	□	▲
Stop	○	□	▲
Stop with errors	○	□	▲
Stop	○	■	▲
System diagnostics	●/○	■/□	▲/▲
Battery fault	○	□	▲/▲

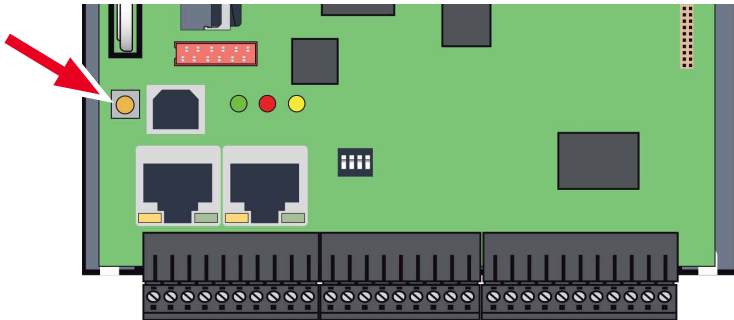
Key:

- LED off
- LED on
- /○ LED blinks

Start	Self-diagnosis for approx. 1 sec. after switch on or restart
Run	Normal processing of the user program after start-up.
Run conditional	Conditional Run status A condition was set in the debugger (Run until...), which has not been fulfilled yet
Run with error	The same as Run, but with an error message
Run conditional with error	The same as Run conditional, but with an error message
Stop	The status Stop occurs in the following cases: <ul style="list-style-type: none"> - Programming unit connected in PGU mode while the CPU was switched on - PGU stopped by programming unit - Condition for BED.RUN was fulfilled
Stop with error	The same as Stop, but with an error message
Halt	The status Halt occurs in the following cases: <ul style="list-style-type: none"> - Stop instruction processed - Serious error in the user program - Hardware fault - No program loaded - No communications mode on the S-bus PGU or Gateway Master Port
System diagnostics	
Battery fault	Flashes at interval of 500 ms
Reset	The RESET status has the following causes: <ul style="list-style-type: none"> - Supply voltage too low - Firmware not started

3.8 Run/Stop Button

The operating mode can be changed during operation or during power-up:



3

During power-up

If the Run/Stop button is pressed during power-up of the PCD and then released during one of the sequences describe below, one of the following actions can be triggered:

LED sequence	Action
Orange	none
Green, blinking (1 Hz)	Switches to "Boot" status and waits for FW download.
Red, blinking fast (4 Hz); FW > V 01.08.45	The system starts in the same manner as for an empty SuperCap or empty or absent battery. In the process, media/resources (flash, registers, flags, etc.), user program and hardware settings are deleted. The time is set to 00:00:00 01/01/1990. The backup of the on-board flash is NOT deleted.
Red, blinking slowly (2 Hz)	The PCD does not start up and switches to "Stop" mode.
Red/Green, blinking (2 Hz)	Saved data is deleted, which means media/resources (flash, registers, flags, etc.), user program, hardware settings and the backup on the on-board flash. If a plug-in flash card (see chapter "3.5 System Memory Structure") was used, its program is not copied to the on-board flash.

During operation

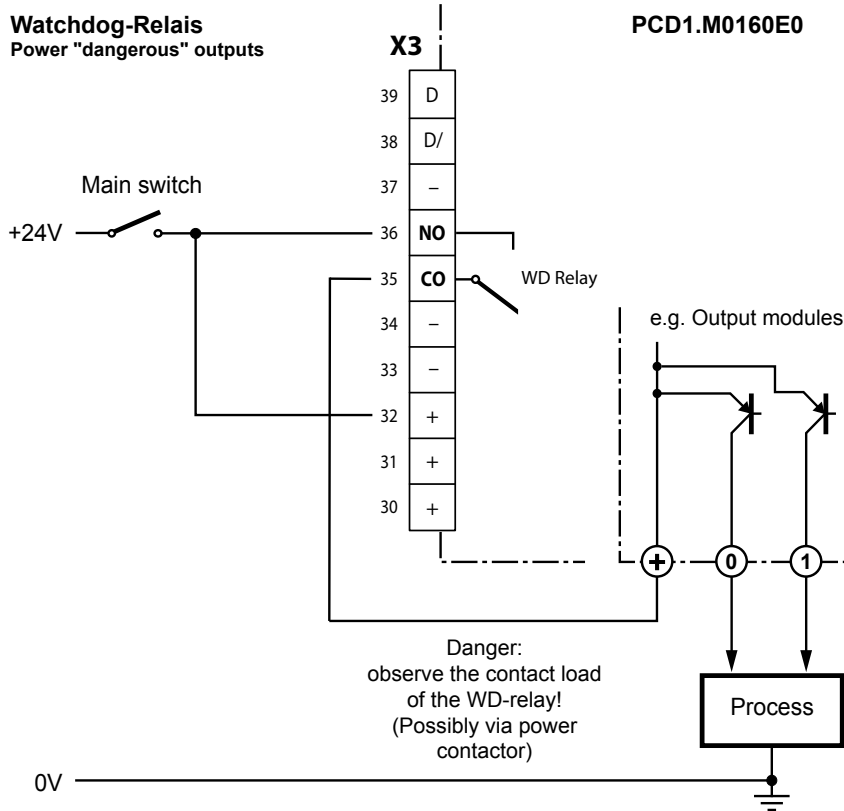
If the button is pressed in Run mode for longer than 1/2 second and less than 3 seconds, the controller switches to Stop mode and vice versa.



If the button is pressed for longer than 3 seconds, the last saved user program is loaded from the flash memory.

3.9 Watchdog (Hardware Relay)

PCD1.M0_CPU's have a hardware watchdog as standard equipment. The watchdog relay is at Pins 35 and 36 at Plug X3



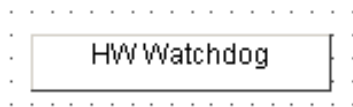
3

Functional description

As soon as the watchdog relay is called at the address O 255 by a switch on/off frequency of < 200 ms, the relay contact closes. It remains closed until the pulse time exceeds 200 ms.

If this happens, it can mean the following:

- ➔ The CPU has stopped
(no longer in RUN mode)
- ➔ Program execution too long
(AWL program loops, program too large)

Example FUPLA FBox:

Further details are available in the online help of the FBox "HW watchdog"

3

Example of an instruction list (IL) sequence:

Label	Com- mand	Operand	Comment
	COB	0 0	; or 1 ... 15
	STL	WD_Flag	; Helpsflag invers
	OUT	WD_Flag	
	OUT	0 255	; Output 255 blinking
	ECOB		

With this code the watchdog triggers even for (continuous) loops that are due to programming. Regarding user program cycle time, please note the following:



With cycle times longer than 200 ms, the code sequence must be repeated multiple times in the user program in order to prevent the watchdog triggering during RUN.

Since address 255 falls outside the normal I/O range of a PCD1.M0_, there are no limitations on permissible I/O modules.

3.10 Watchdog (Software)

The hardware watchdog offers maximum security. A software watchdog can be sufficient for non-critical applications, whereby the processor monitors itself and the CPU is restarted in the event of a malfunction or a loop. The core of the watchdog software is the instruction SYSWR K 1000. The watchdog function is activated when this instruction is output for the first time. It must then be output at least every 200 ms, otherwise the watchdog will be triggered and the PCD restarted

3

Instruction in IL code:

Label	Command	Operand	Comment
	SYSWR	K 1000	; Software watchdog instruction
		R/K x	; Parameter according to the following ; table ; K = Constants on ; R = Register ; Blank space ; x = 0 The software watchdog is deactivated. ; x = 1 The Software Watchdog is activated if the instruction is not repeated within 200 ms, a cold start is performed. ; x = 2 The Software Watchdog is activated if the instruction is not repeated within 200 ms, XOB 0 is called, then a cold start is performed.

“XOB 0” calls are entered in the PCD History as follows:

- «XOB 0 WDOG START» if XOB 0 was triggered by the watchdog software
- «XOB 0 START EXEC» if XOB 0 was triggered by a power supply error

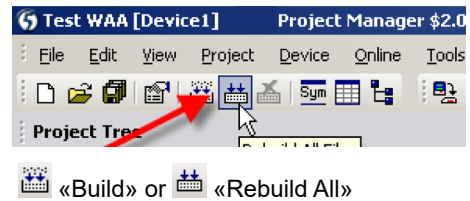
3.11 Program Download and Backup

3.11.1 User Program Download to PCD1 with PG5®

1 Creating and compiling the user program

After successfully compiling the project without errors, the file with extension “.pcd” contains the following information:

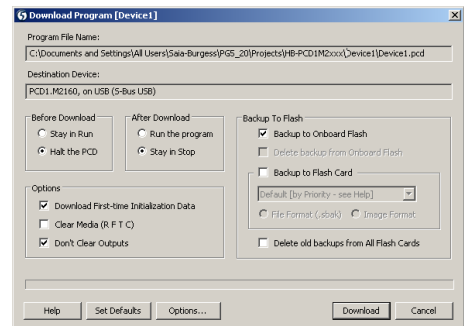
- User program (FUPLA, IL, etc.)
- Configuration files (BACnet, LON, etc.)
- Data for the initialisation of resources for the first time



3

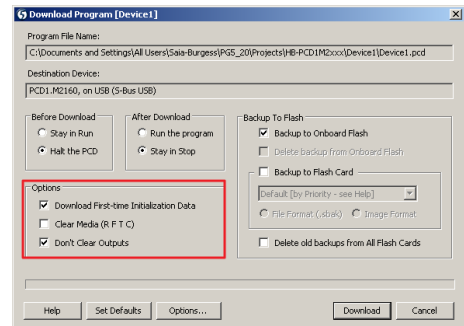
2 Program download

“Download” in the SPM opens the window opposite. If all settings are as desired (see below), the user program is loaded into the PLC with the “Download” button.



3 “Options” area

- | | |
|---|--|
| Download First-time Initialisation Data | Initialisation of media (registers, flags, etc.) for the first time |
| Clear Media (R, F, T, C) | All media, such as flags and registers are set to zero. Including all media for media mapping. |
| Don't Clear Outputs | Physical outputs with or without media mapping save their values while the new program is transmitted to the execution memory. |

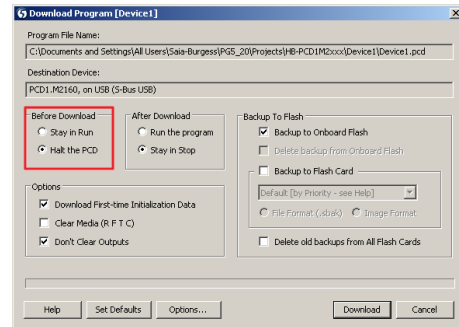


4 “Before download” area

Two options are available before the downloading of the user program file:

Stay in Run Remain in Run The file is downloaded to the file system while the PLC is in RUN. The PLC first stops the successful download, parses the file and performs a restart.

Stop in PCD First the PLC stops, then the file is downloaded to the file system. After the successful download, the PLC parses the file and performs a restart.



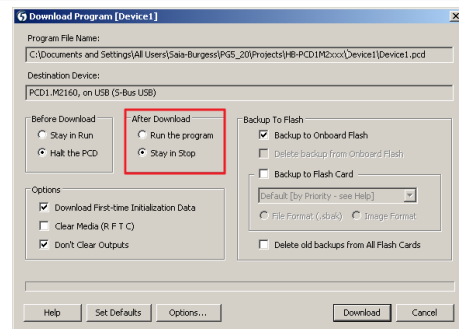
3

i The PLC switches to STOP for the parsing of the new file. This step takes 2 to 5 seconds, depending on the size of the user program.

5 “After download” area

Run the program Sets the PLC to RUN, once the download is successfully completed

Stay in Stop After the download, PLC remains in STOP



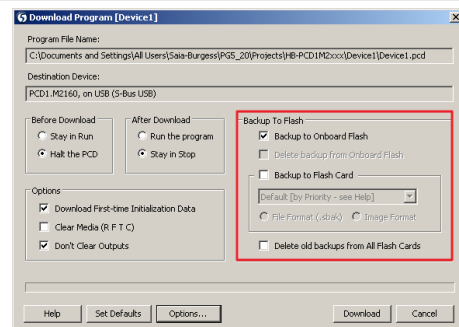
6 “Backup to Flash” area

Backup to on-board flash Physical outputs with or without media mapping save their values while the new program is transmitted to the execution memory.

Delete backup from On-Board Flash All media, such as flags and registers are set to zero. Including all media for media mapping.

Backup to Flash Card Save to flash card

Delete old backups from All Flash Cards Deletes old saved programs from all flash cards



7 “Download” button

- | | |
|------------------|---|
| “Security” area | <ul style="list-style-type: none">- Warn if PCD contains program with different name- Warn if different Station number or IP address- Warn if a running program will be restarted/stopped- Verify PCD Serial Number ...
Warning: The PCD already contains another program- Show Program Information before downloading
Warning: The PCD already contains another program- Warn if LON Bindings may be lost
Warning: The PCD already contains another program |
| “Behaviour” area | <ul style="list-style-type: none">- Download automatically after successful build- Download program only if changed- Go online after successful download (observation mode) |

3



It is not possible to download only those blocks which have been modified. The user program is downloaded into the on-board memory in a file and, after a restart of the system, the process is complete. If the download is not successfully completed, the FW deletes all files within the system folder.

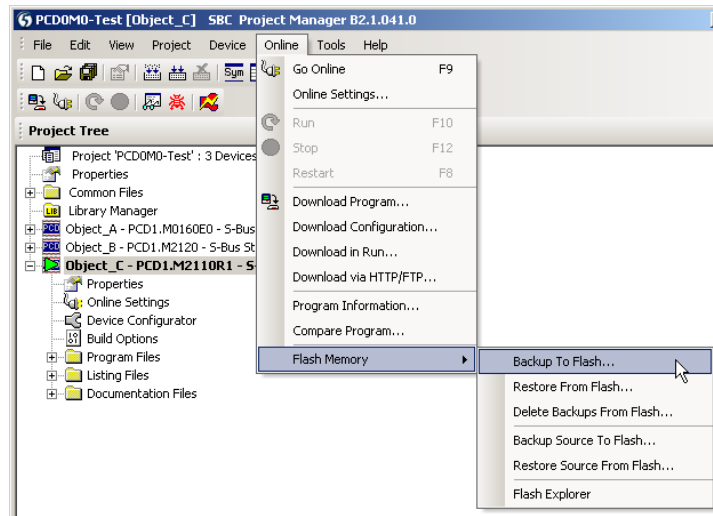
Once the download has been successfully completed, start the PCD:

After the system restart, the user program and ROM DB/text are transferred into the execution memory. This is a write-protected memory, which does not need to be backed up; all data is stored in the PCD file system.

3.11.2 Backup and Restore User Program

Backup with Saia PG5®

Select a backup with
“Copy program to flash...”



3

Since the user program is already stored in the on-board flash memory, only the RAM DB/text data from the on-board flash memory is backed up in the folder PLC_SYS. This folder is not visible for the user. Access is not permitted.



Registers, flags, timer and counters are not saved in this manner.

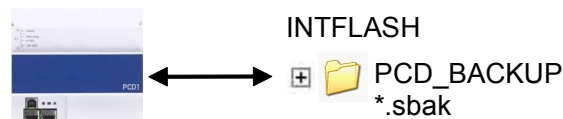
During a restore, the text/DB data is copied back into the SRAM memory.

Backup to the INTFLASH file system

In order to be able to use backup/restore with internal flash, a PCD_BACKUP folder must be created.

RAM DB/text data is stored in the internal PCD_Backup folder.

This allows the backup files to be accessed via the FTP server and then uploaded to a PC.

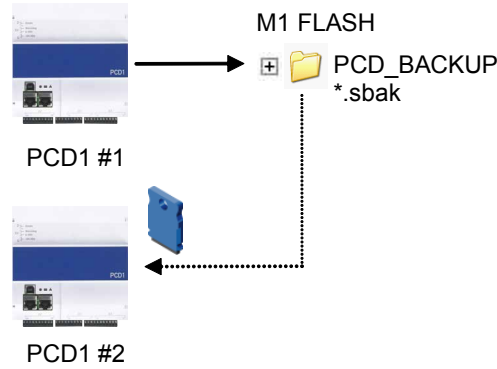


Backup to flash memory modules

For the use of “backup/restore” on the internal FLASH, a folder name PCD_ BACKUP must be created.

Backup to M1 flash
Please note that the M1 flash must be deleted beforehand.

When using use of the backup function to M1 modules, no other files should be written to the module.



3

Please note that a 512 kByte user program and 128 kByte RAM DB/text will generate a file of approximately the same size.

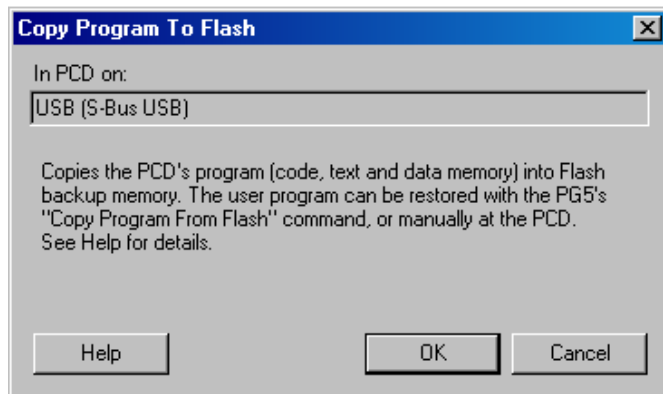


Limitations:

Files generated cannot be copied directly from one folder to another! These files may not be deleted from the original folder or renamed. If they are, the restore function will no longer work correctly in this case!

The following window will appear.

Click OK to start the backup process.



Restoring user program and DB/text

Two options are available:

- With the PG5 under “Online → Flash memory → Restore source of flash” or
- By pressing the “Run/Stop” button for at least 3 - 5 seconds in RUN mode.
ATTENTION: If the button is pressed for longer than 10 seconds, there is the risk of resetting the system and/or deleting the memory.

3

The CPU searches memory locations for backup files in the following order:

1. M1 Flash
2. INTFLASH
3. PLC_SYS

4 Inputs and Outputs

This chapter describes the inputs and outputs of the PCD1.M2_ in terms of their function and pin assignment.

Three possible locations for inputs and outputs are described. Optional extension can be use external RIOs.

4

4.1 On-Board

On-board means mounted “on the CPU mother-board”

4.1.1 Connection overview

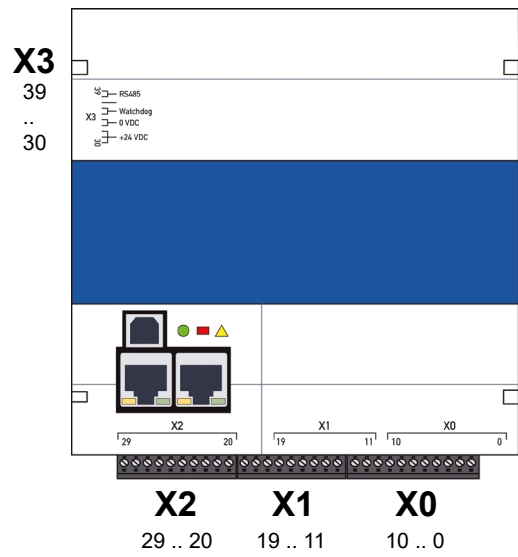
X0		
0	PGND	
1	Uext	+24 V external
2	PWM0	PWM0 or Output 8
3	Out 0	Output 0
4	Out 1	Output 1
5	Out 2	Output 2
6	Out 3	Output 3
7	IO4	Input or Output 4
8	IO5	Input or Output 5
9	IO6	Input or Output 6
10	IO7	Input or Output 7

X1		
11	In 0	Input 0
12	In 1	Input 1
13	In 2	Input 2
14	In 3	Input 3
15	IX0	Interrupt or Input
16	IX1	Interrupt or Input
17	AGND	
18	AIN0	Analogue Input 0
19	AIN1	Analogue Input 1

X2						
	PCD7.F121S	PCD7.F110S	PCD7.F180S	PCD7.F150S	PCD7.W600	
	RS-232	RS-485	RS-422	Belimo	RS-485 isol.	4xAO (0..+10V)
20	PGND	PGND	PGND	PGND	PGND	PGND
21	TxD	Rx-Tx	Tx	MP	Rx-Tx	A0+
22	RxD	/Rx-/Tx	/Tx	“MFT“	/Rx-/Tx	A0-
23	RTS		Rx	“IN“		A1+
24	CTS		/Rx			A1-
25	PGND	PGND	PGND	PGND	PGND	PGND
26	DTR		RTS			A2+
27	DSR		/RTS			A2-
28	COM		CTS		SGND*	A3+
29	DCD		/CTS			A3-

* SGND is signal return for Rx-Tx-/Rx-/Tx signals and is isolated from PGND

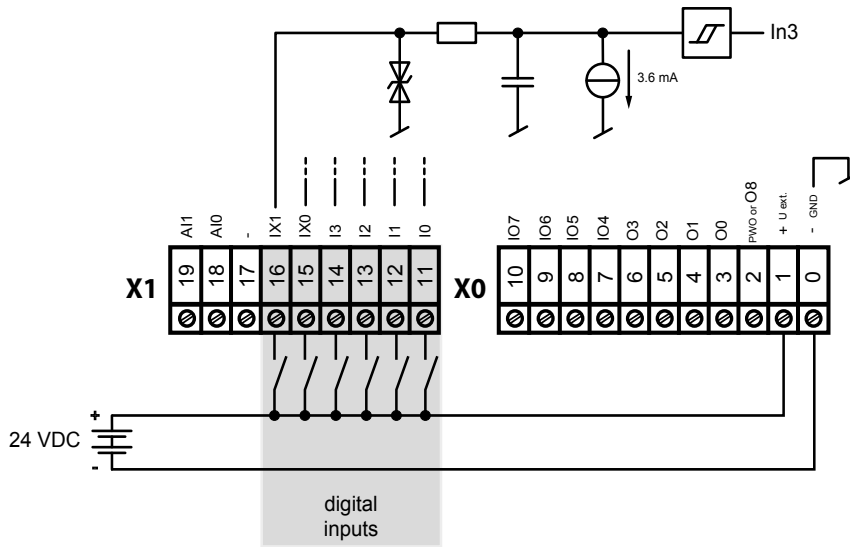
X3		
30	+	+24 VDC
31	+	
32	+	
33	-	0 VDC
34	-	
35	WD	Watchdog relay or Output 9
36	WD	Watchdog relay
37	-	PGND
38	/D	RS-485 up to 115.2 kbit/s
39	D	Profi-S bus up to 187.5 kbit/s



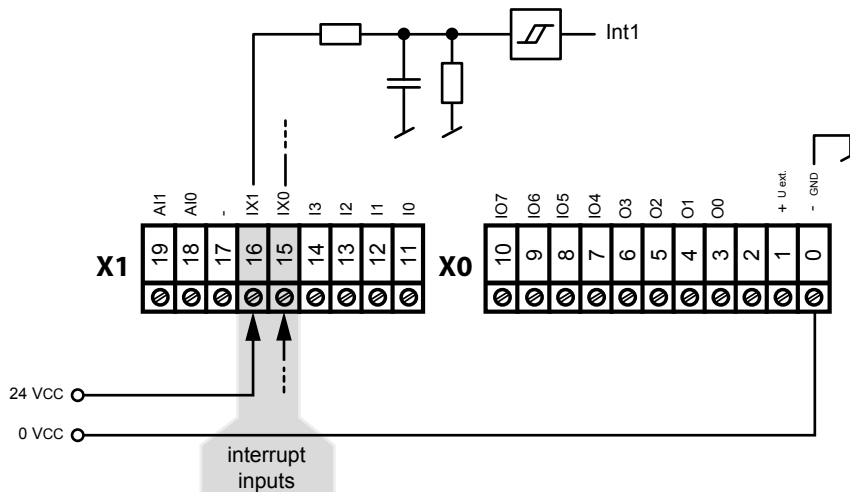
4

4.1.2 Digital Inputs (Terminal Block X1)

Number of inputs	4, source operation, electrically connected
Input voltage	Typ. 24 VDC (15...30 VDC)
Input current	Typ. 3.6 mA at 24 VDC
Input delay	Typ. 3 ms
Surge protection	No
LED	No
Terminals	Plug-in screw terminal block



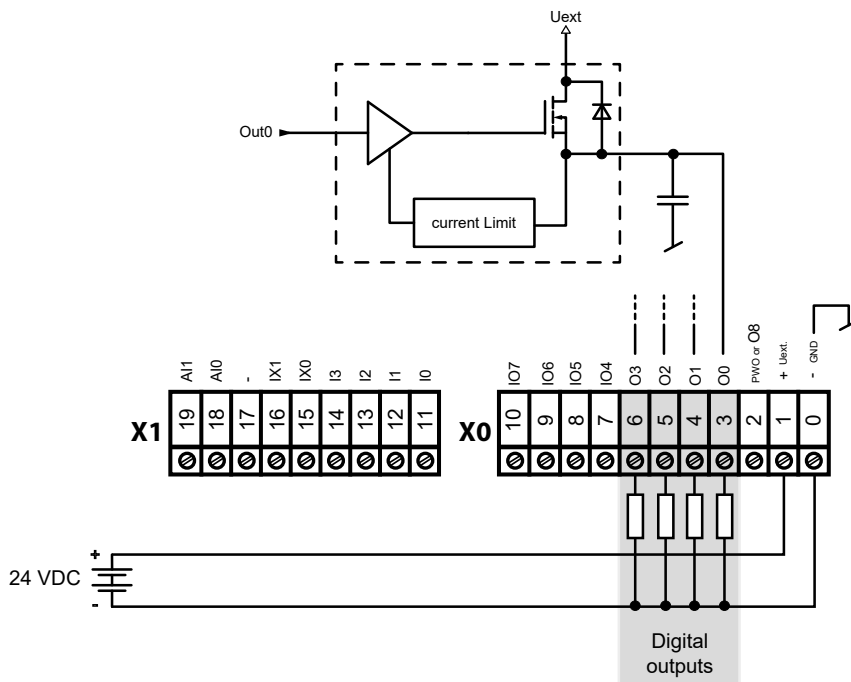
The terminals No. 15 and No. 16 can be used as an input or as an interrupt (see Section 4.1.7).



Input signals (always source operation):
 H = 15...30 V
 L = - 30...+ 5 V or unconnected

4.1.3 Digital Outputs (Terminal Block X0)

Number of outputs	4
Voltage range	24 VDC (12...32 VDC) smoothed
Output current	Max. 0.5 A
Output delay	typ. 50 μ s, max 100 μ s at ohmic load
Contact protection	Transistors
LEDs	No
Connections	Plug-in screw terminal block



4.1.4 Digital Inputs and Outputs (Terminal Block X0)

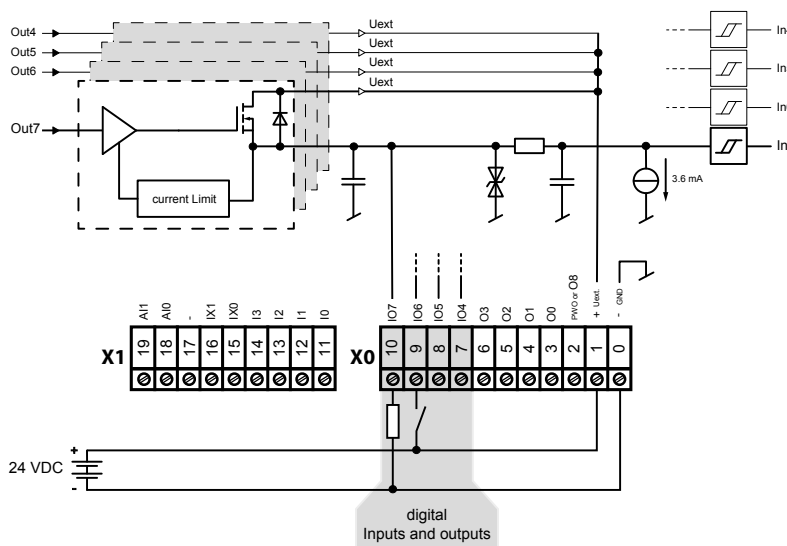
Terminal numbers No. 7 to No. 10 on Terminal Block X0 can be used as either inputs or outputs. Configuration takes place in the Device Configurator. Depending on the configuration, the technical data corresponds to that of a normal digital input or output:

Configured as an input:

Input type:	Source operation, electrically connected
Input voltage:	Typ. 24 VDC(15...30 VDC)
Input current:	Typ. 3.6 mA at 24 VDC
Input delay:	Typ. 3 ms
Surge protection:	No
LEDs	No
Connections	Plug-in screw terminal block

Configured as an output:

Short-circuit protection	Yes
Voltage range	24 VDC (12...32 VDC) smoothed
Output current	Max. 0.5 A
Output delay	Typ. 50 μ s, max 100 μ s at Ohmic load
LEDs	No
Connections	Plug-in screw terminal block



NOTE: Subject terminal block X0

The terminal Uext serves to feed the outputs to terminals 7 ... 10th

If at least I/O 4 ... 7 operated as a receipt, the following must be considered:

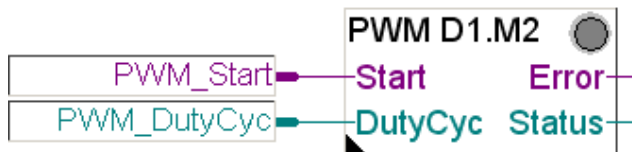
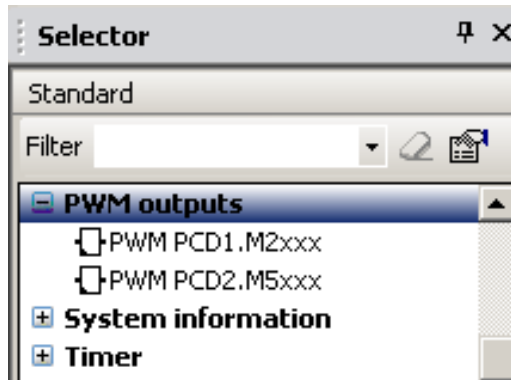
If this external supply U ext which outputs the power off and the inputs I/O 4 ... 7 is still tension on the supply voltage of the outputs O 0, ... 3 and I/O 4 ... 7 via the built-in output transistor of the I/Os diode fed back and would feed the device connected to the output load.

4.1.5 PWM Output (Pulse width modulation) (Terminal Block X0)

Terminal no. 2 on Terminal Block X0 can be used either as a normal, digital output or as a PWM output. Configuration takes place in the Device Configurator.

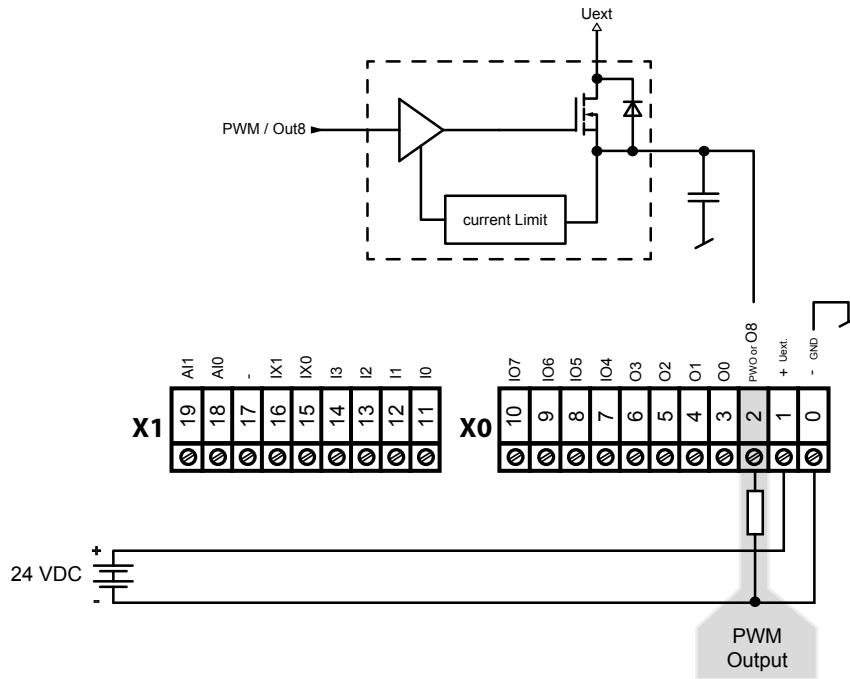


There is an FBox for the using of the PWM output.

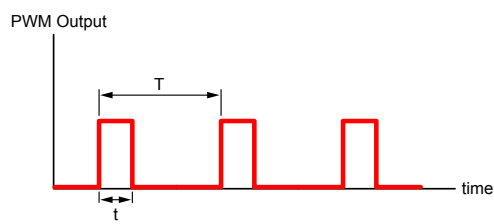


Number of PWM outputs:	1
Voltage range	24 VDC (12... 32 VDC) smoothed
Output current:	Max. 0.2 A
Adjustable frequencies	1 Hz, 4 Hz, 15 Hz, 30 Hz, 61 Hz, 122 Hz, 244 Hz, 488 Hz, 975 Hz, 1950 Hz
Duty cycle range	0-100 %
Terminal:	Plug-in screw terminal block

Maximum operating frequency is 2 kHz (rise and fall times are 20 µs).



4



Frequency = $1/T$
 Duty Cycle = t/T

4.1.6 Interrupt Inputs (Terminal Block X1)

Basic principle

Due to the input filter and the effect of the cycle time, the digital input modules are not suitable for reacting immediately to events or fast computing processes. Some CPUs have interrupt inputs for this purpose.

If a positive flank is detected at an interrupt input, the corresponding XOB (e.g. XOB 20) will be called. The code in this XOB defines how the unit should react to the event, e.g. increment a counter.

4



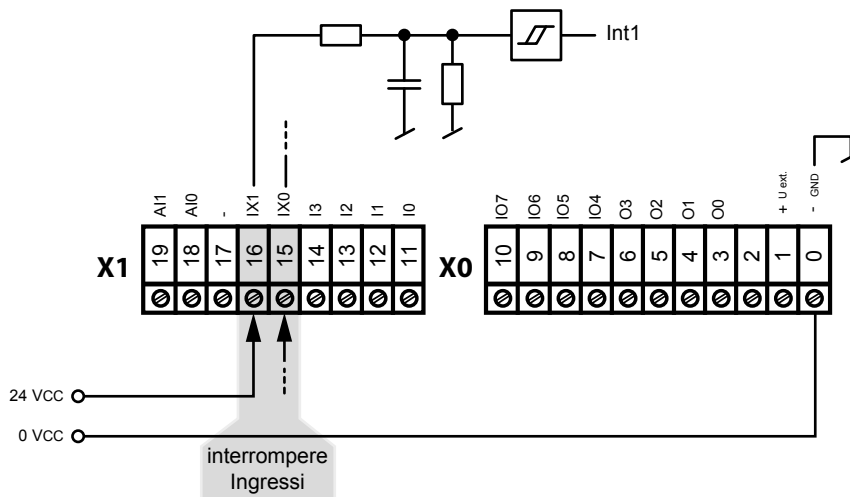
The code in XOBs, which is called by interrupt inputs, must be as short as possible so that sufficient time remains between the interrupts in order to process the rest of the user program.



Many FBoxes are intended for cyclical calling and are not suitable for use in XOBs, or are only suitable to a limited extent. Exception: The FBoxes of the Graftec family (standard library) are well-suited.

PCD1 Interrupt Inputs 24 VDC

Both interrupt inputs are located on the main circuit board and can be connected through the 9-pin plug-in Terminal Block X1 (Terminals 15 and 16). Source operation is always used.



I segnali di ingresso (sempre logica positiva): H = 15...30 V L = - 30...+ 5 V o non collegato

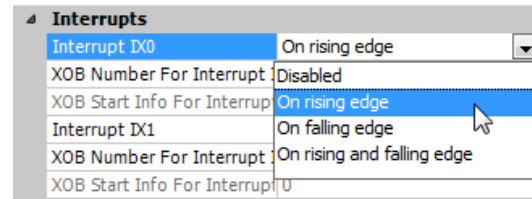
Interrupt assignment

Terminal	Caption	Interrupt	Called XOB
15	IX0	Int0	XOB 20
16	IX1	Int1	XOB 21

Signal edge selection

The signal edges that causes the associated XOB to be called is selected as follows:

- PG5 Device Configurator
- Onboard In-/Outputs
- Properties
- Interrupts



4

Operation IX0 (also applies for IX1)

With a positive flank at Input IX0, XOB 20 is called. The maximum reaction time until the call of XOB 20 is 1 ms. The code in this XOB defines how the system should react to the events, e.g. by increment a counter (max. input frequency 1 kHz, whereas the pulse/pause ratio is 1:1, maximum sum of the two frequencies is 1 kHz).

4.1.7 Analogue Inputs (Terminal Block X1)

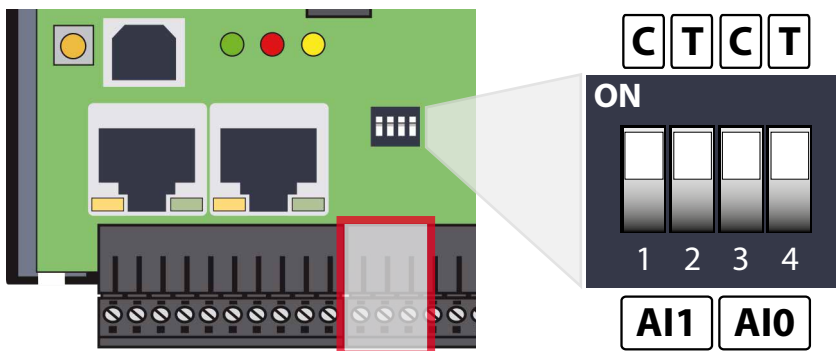
Number of inputs:	2
Galvanic separation	No
Signal ranges:	-10...+10 V (12 bit + prefix) -20...+20 mA (12 bit + prefix) RTD (12 bit)
Connection technology for sensors	2-wire (passive input)
Measurement principle:	One-sided
Input resistance:	±10 V Range: 240 kΩ ±20 mA Range: 125 Ω
Input filter:	typ. 5 ms
Input range for temperature sensors	PT1000: -50...+400 °C NI1000: -60...+200 °C NI1000 L&S: -30...+140 °C Resistance 0...2.5 kΩ
Precision at 25 °C:	± 0.5 %
Temperature sensor(0...+55°C):	± 0.25 %
Overload protection:	±10 V Range: ± 35 V (39 V TVS diode) ±20 mA Range: ±40 mA
LED	No
Terminals	Plug-in "pressure" 10-pin terminal block, 3.5 mm for wiring up to 1 mm ²



On delivery, preconfigured for NI1000.

Configuration of the analogue input channels:

As shown in the following illustration, the analogue input range is selected with configuration switches.



		U	C	T
AI0	SW1	3 OFF4 OFF	3 ON4 OFF	3 OFF4 ON
AI1	SW1	1 OFF2 OFF	1 ON2 OFF	1 OFF2 ON

The following ranges are supported:

Voltage	±10 V	Both switches off (see Channel 0 configuration above)
Current	±20 mA	Switch "C" on, switch "T" off (see Channel 1 configuration above)
Temperature/resistance		Switch "T" on, switch "C" off (see Channel 2 & 3 configuration above)

Definition for range, over-range/under-range and status flag:

Temperature inputs:

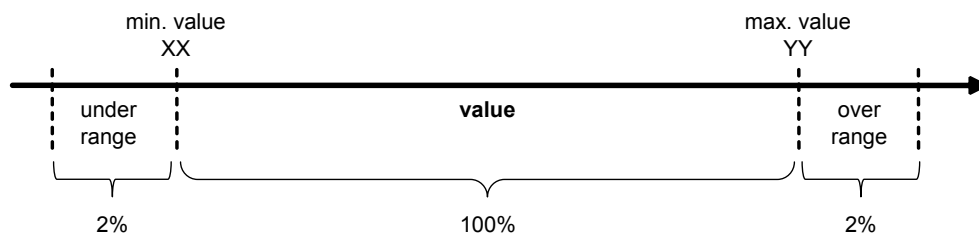
Model	min./max. Status flag	Value Range
Pt 1000 (-50...400 °C)	-500 / 4000	Limits -500...4000
Ni 1000 (-50...210 °C)	-500 / 2100	Limits -500...2100
Ni 1000 L&S (-30...140 °C)	-500 / 1400	Limits -300...1400

Each time the min./max. values are reached, the min./max. status flag is set.

Resistance, voltage and current inputs: The overall value range is defined by the range type:

Model	min./max. Status flag	Range of the calculated values
Resistance 0...2500 Ω	0...25000 Min. Flag not set	Limit exceeded 25500 (25000+2 %)
Voltage input (-10...+10 V)	Xx / yy	102 % of the defined range
Current input (-20...+20 mA)	Xx / yy	102 %

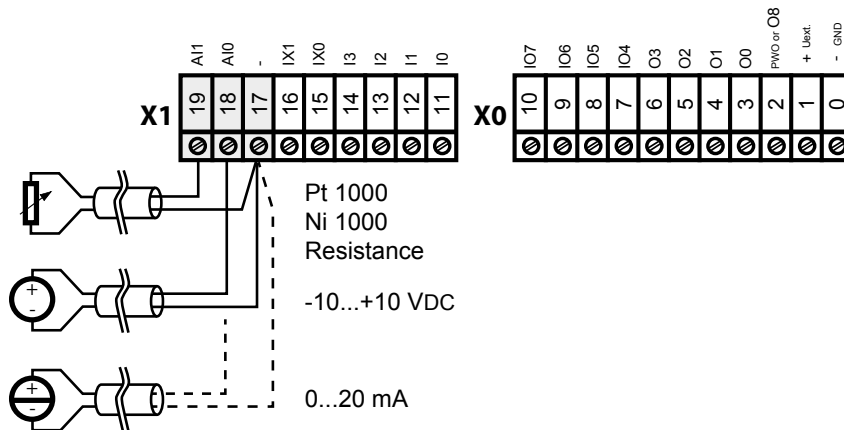
Each time the min./max. values are reached, the min./max. status flag is set.



The status flag remains set until the status has been read. With media mapping the status flag is read at the end of each COB. This means that the status flag is reset at the end of each COB.

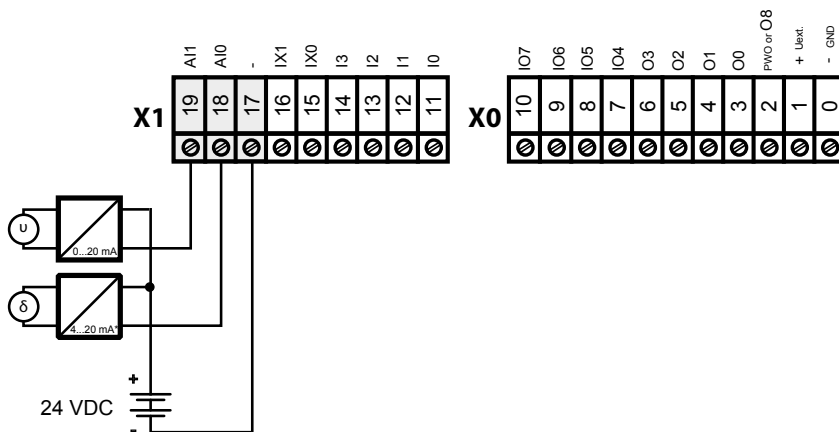
With direct access, the status flag is reset as soon as the user program reads the status flag.

Connection concept



4

Connection concept for two-wire transmitters



* 4..20 mA through the user program
 or in the Saia PG5® → Device Configurator → Media Mapping

4.2 Plug-In I/O Module for slot A

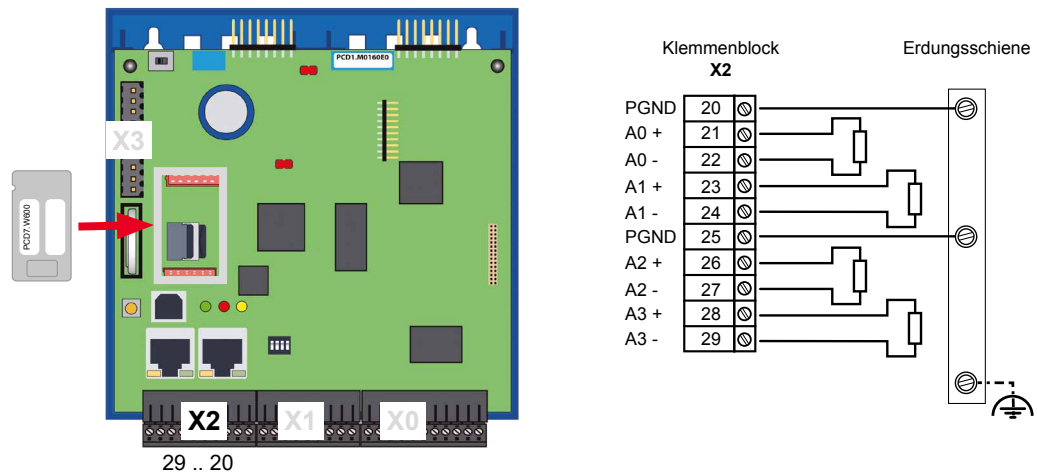
4.2.1 Analogue outputs

PCD7.W600 4 analogue outputs with 12 bits resolution

This analogue outputs module (0 to +10 V) can be plugged on the socket A of a PCD1.M2_ / .M0_ instead of a communication interface.

The configuration of the outputs takes place in the Device Configurator like on-board I/O's

4



General specifications

Technical data	
Module compatibility	PCD1.M2xxx, PCD1.M0160E0, PCD1.M2110R1
Module current consumption	V+ 25 mA / +5 V 30 mA
Number of outputs	4
Terminals	1 plug-in screw terminal block, 10-pole, 3.5 mm for wiring up to 1 mm ²
Isolation	No isolation between channels and/or PCD
Output signal range & resolution	With D/A converter 12 bits Nominal range: 0...+10 V Resolution 2.6 mV of least significant bit (LSB)
Monotonicity	Yes
Output impedance (max.)	0.7 Ω
Allowable load resistance	≥3 kΩ
Allowable capacitive load	≤20 nF
Allowable types of load	Floating or grounded (the minus of the outputs is internally connected with the PCD ground)
Short-circuit protection	YES permanent
Accuracy @25°C	±0.2 % of the full scale (10 V)
Temperature coefficient	±100 ppm/K of the full scale (10 V)

Accuracy over full temperature range (0..+55°C)	±0.5 % of the full scale (10 V)
Maximum temporary deviation during electrical interference test	±0.2 % of the full scale (10 V) for fast transient burst (EN 61000-4-4) & for radiofrequency interference (EN61000-4-6)
Settling time for full-range change	≤5 ms
Overshooting	±0.1 % of the full scale (10 V)
Scaling (PG5)	0..4095, 0..10000 or user defined

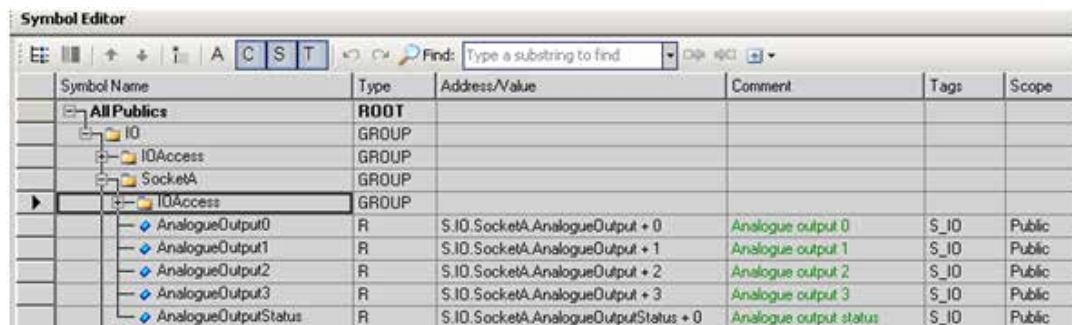
Prerequisite

PCD firmware version 1.23.39 or higher

PG5 version 2.1.300 or higher

Programming with media mapping

When the media mapping is enabled, each module has these following registers:



The analogue values shall be directly written in the AnalogueOutputx registers. Each channel will be updated after the last COB.

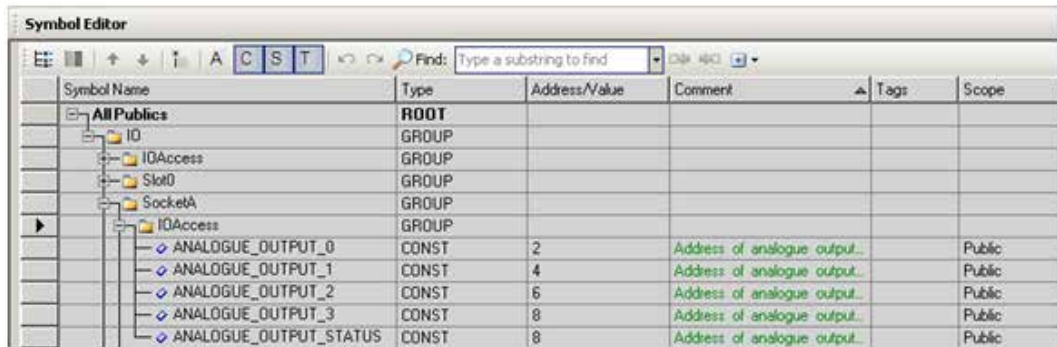
The status register is updated before the first COB is executed.



When using media mapping, it is not possible to detect which channel has not been updated in case of error in the status register.

Programming with direct access

The module allows direct access with WRPW commands.



4

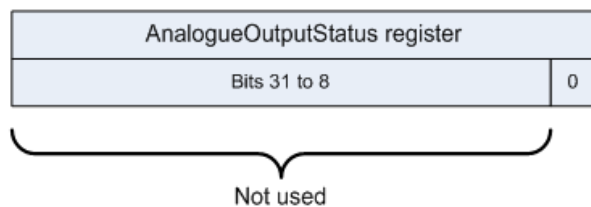
Here an IL program example to write an analogue value to the output0 and to read the diagnose register.

```

WRPW  IO.SocketA.IOAccess.ANALOGUE_OUTPUT_0
R 99

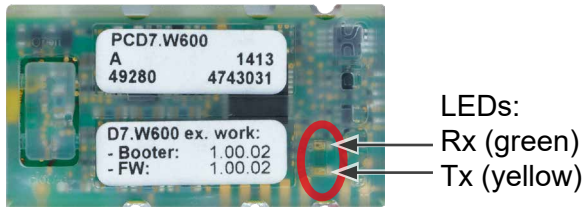
RDPB  IO.SocketA.IOAccess.ANALOGUE_OUTPUT_STATUS
R 100
    
```

With direct access, it is possible to know which channel has not been correctly updated if the status register is read direct after the Write command.



Bit	Status	Description
0	1	if a communication error has been detected (between PCD and module)This bit is automatically cleared when the status register is read

LEDs and his Importance



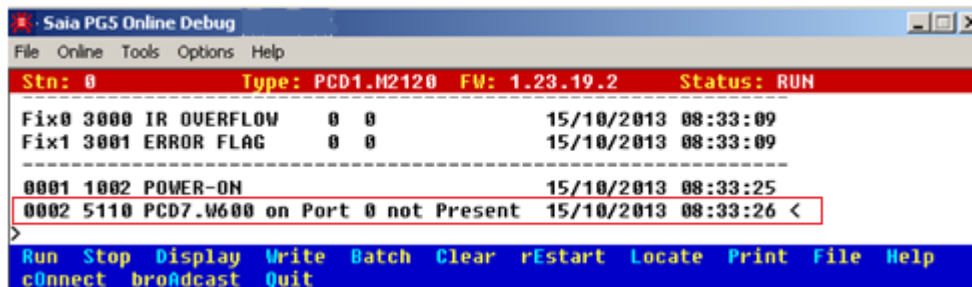
The LEDs Rx/Tx blink when the module is communicating with the PCD.

4

- They can be permantly activated if media mapping is used or
- Shortly blink with direct access.

Module detection

If the module is not plugged, there is a history entry.



If you need to detect if the module is plugged or not in your program code, you can use the following function:

```
CSF S.SF.SYS.Library ;Library number
S.SF.SYS.ReadDeviceInfo ;Read Device Information
K 2 ;1 R|K IN, Device Port (1 IO Bus 2 Extension)
K 22 ;2 R|K IN, Device ID
K 0 ;3 R|K IN, Slave ID
RStatus ;4 R OUT, Status
TASN ;5 TEXT OUT, ASN
THWVrs ;6 TEXT OUT, HW version
RHWModif ;7 R OUT, HW modif
TFabDate ;8 TEXT OUT, Fabrication Date (ww/yy)
RSerNum ;9 R OUT, Serial Number
TFWVersion ;10 TEXT OUT, FW version
```

If the module has been correctly plugged, the status value is a positive number and all device information can be read. If the module has not been correctly plugged or simply not plugged, the returned value is negative.

4.3 RIO

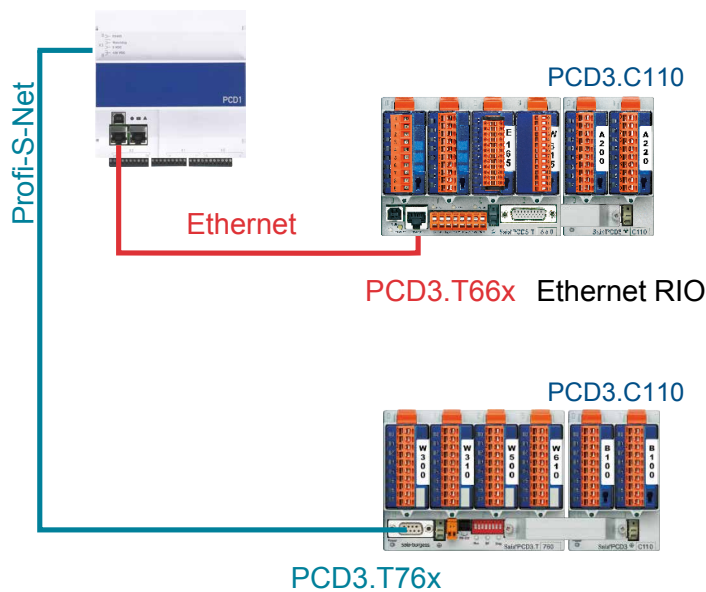
For the decentral extensions with inputs and outputs via Profibus or Ethernet, the PCD3.RIO (Remote I/O) modules are recommended (see also Manual 26-789).

PCD3.T760 Integrated Profibus DP slave / Profi S-Net slave connection up to max. 187.5 kbit/s 4 plug-in I/O modules Integrated webserver for diagnostics, support and commissioning (connection to PC via optional PCD3.K225 connection cable)

PCD model	Max. number of PCD3 I/O
PCD3.T760 RIO nodes	256 per node

PCD3-RIOs are used to detect decentral I/O signals. PCD3.RIOs can communicate with all master PCD via Profibus DP; this can take place through the integrated Profi-S I/O on the PCD1.M2_.

A detailed description is found in Section 4 of the PCD3 manual 26-789.



Expansion of the PCD1.M0160E0 is possible with PCD3.T66x and PCD3.T76x RIO modules.

5 PCD1.M0160E0 Communications Interfaces

The word “port” will be used for the remainder of this manual instead of “communications interface” for the purpose of simplification.

Using the SBC S-Bus



SBC S-Bus stands for the proprietary communications protocol of Saia PCD®.



The SBC S-Bus is basically designed for communications using the engineering and debugging tools, as well as for connection to management levels/process control systems. It is not suitable or approved for connecting the field devices of other manufacturers. An open, vendor-neutral field bus is more appropriate for this purpose.

5.1 On-board

When we use the term “On-board”, we mean the CPU board. In other words, the term “On-board interfaces” means interfaces already available on the CPU board or in preparation for it.

5.1.1 USB Port (Programming Interface)

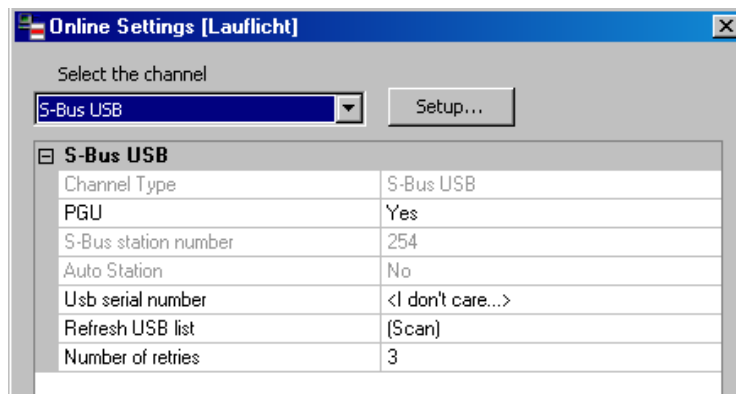


Plug:	Standard vertical USB series B (device plug)
Default :	USB 1.1 device (slave), full speed 12 Mbps, with Softconnect
Protection:	transil
Hardware:	On-board USB 5V supply

5

The USB port is only used as a PGU interface. To use the USB interface, the program package Saia PG5® version 2.0 or later must be installed on the PC.

If the PCD is connected to the PC for the first time through the USB port, the PC operating system (Windows) automatically loads the corresponding Saia PCD® USB driver. To connect the PCD via USB, the following setting is required in the PG5 project folder for the device concerned under “Online settings”:



Activating the “PGU option” ensures that the PCD connected to the PC can be reached directly, independently of the configured S-Bus address.

5.1.2 Ethernet (Port #9)

A new 10/100 Mbits switch, which automatically adapts to the two speeds, is used for these Ethernet connections. Both sockets can be used independently of one another.



ETH1

ETH2

Function: 2 port switch

Jack type: 2 RJ45s vertically positioned, metal housing, 2 LEDs each

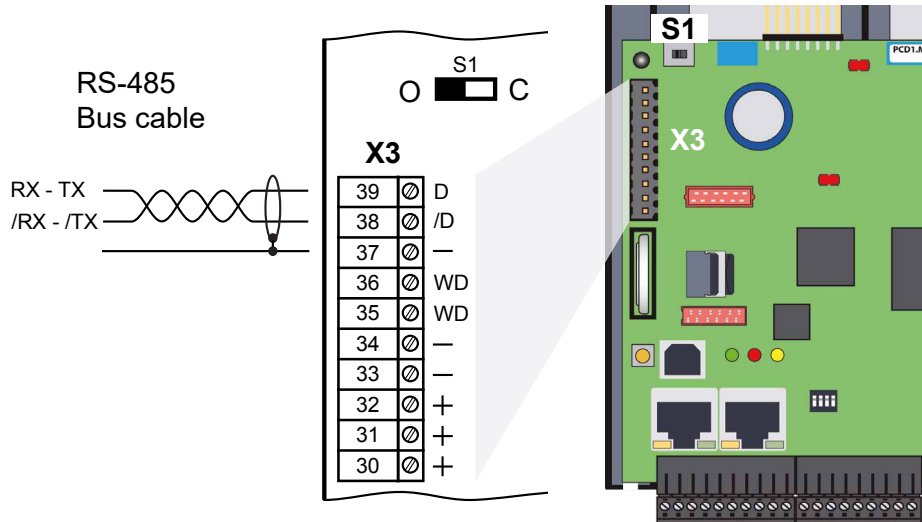
Meaning of the LEDs per jack:

Orange LED Link (connection) and activity

Green LED Speed Off = 10Mbits / On = 100 Mbits

5.1.3 RS-485 (Port #0, not electrically isolated)

In S-Bus, Modbus or MC4 communications mode, an RS-485 link can be established via port 0 with terminal block X3, terminals 38 and 39



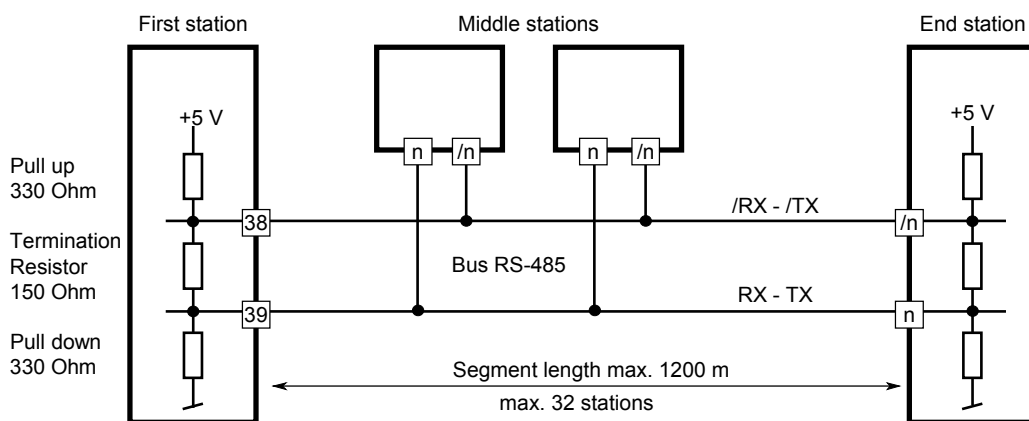
5

Switch S1, connecting or disconnecting the RS-485 termination resistors



With switch S1, the terminating resistors are switched on or off. Switch S1 must be set to “C” (closed) at both outer stations. For all other stations switch S1 remains in the position “O” (factory setting).

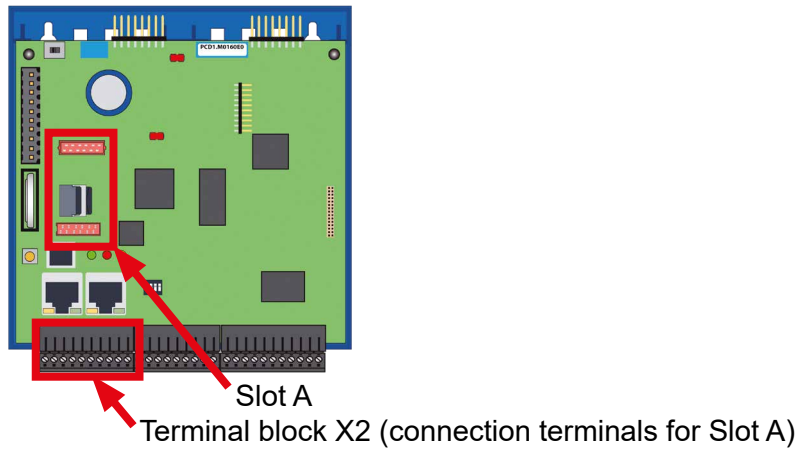
Schematic diagram of an RS-485 bus with terminating resistors.



For more details see in the manual 26-740, Installation components for RS-485 Networks.

5.2 Slot A (Port #1)

Only PCD7.F1xxS modules are supported on the PCD1.M0_.



5



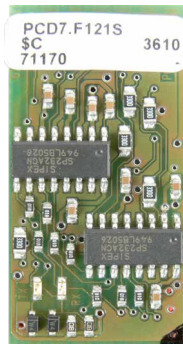
Older interface modules without “S” at the end of the product designation (e.g. PCD7.F110) are not compatible with PCD1.M0_.

Overview of the interface types:

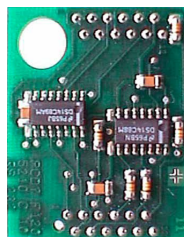
PCD7.F1xxS with housing, 2012 or later



PCD7.F1xxS previous design



PCD7.F1xx not compatible with PCD1.M2_



Important: PCD7.F1xxS devices with hardware version A are not compatible with earlier PCDs (PCD1.M1xx/PCD2.M1xx/PCD2.M48x/PCS1) from NT- based PCD systems.

Malfunction

If interface modules of the PCD7.F1xxS series (hardware version A) are used with the following devices, the interface modules will become hot and their correct function cannot be guaranteed.

- PCD1.M1xx
- PCD2.M1xx
- PCD2.M48x
- PCS

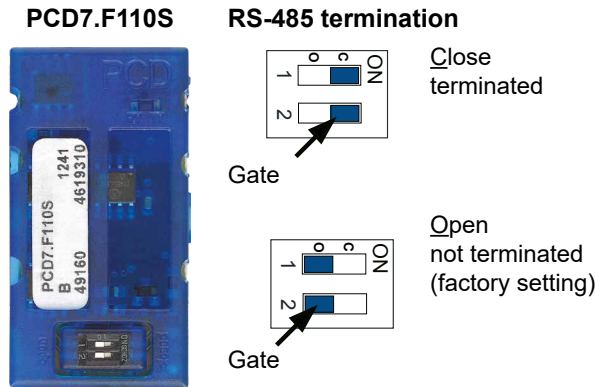
The hardware version can be seen on the white label of a PCD7.F1xxS module in the middle text line.

5

Solution

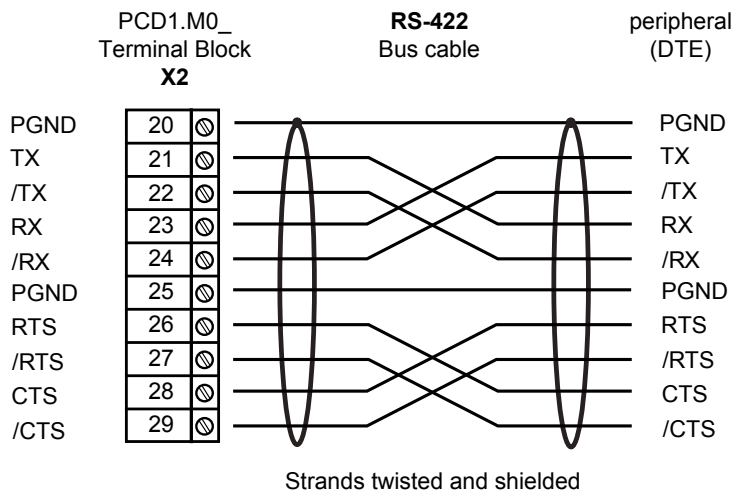
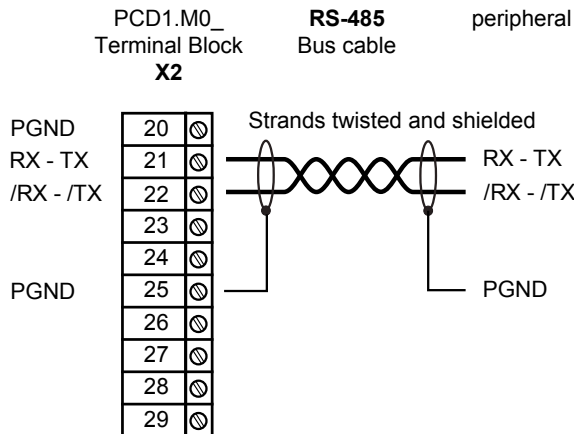
Only use PCD7.F1xxS interface modules PCD7.F1xxS with hardware version B or newer. These are suitable for all PCD generations.

5.2.1 PCD7.F110S Serial Interface Module RS-485/RS-422



5

Plug assignment:



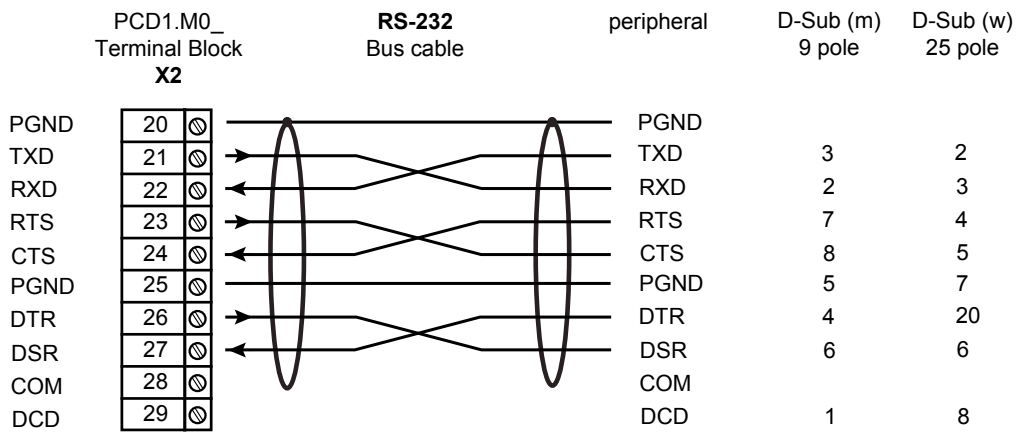
For more details see in the manual 26-740, Installation components for RS-485 Networks.

5.2.2 PCD7.F121S Serial Interface Module RS-232
up to 115 kBit/s, Suitable for Modem Connection

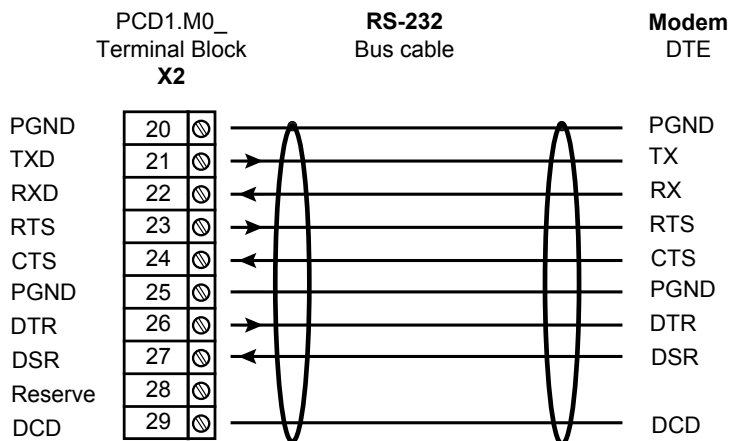
PCD7.F121S



Standard Cabling:

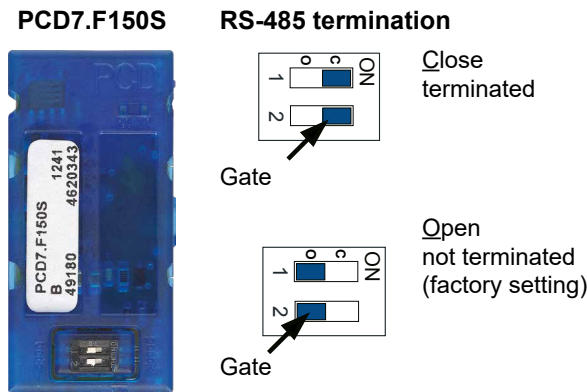


Cabling for Modem connection:



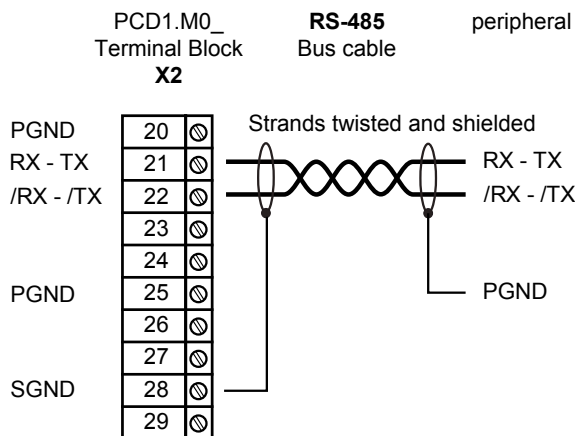
5.2.3 PCD7.F150S Serial Interface Module RS-485 with Electrical Isolation

Electrical isolation is achieved with three optocouplers and a DC/DC converter. Data signals are protected against overvoltage with an anti-surge diode (10 V). Termination resistors can be connected (CLOSED) or disconnected (OPEN) with a jumper.



5

Cabling:



With the use of this module, the permissible ambient temperature is reduced by 5°C.

For more details see in the Manual 26-740, Installation components for RS-485 Networks.

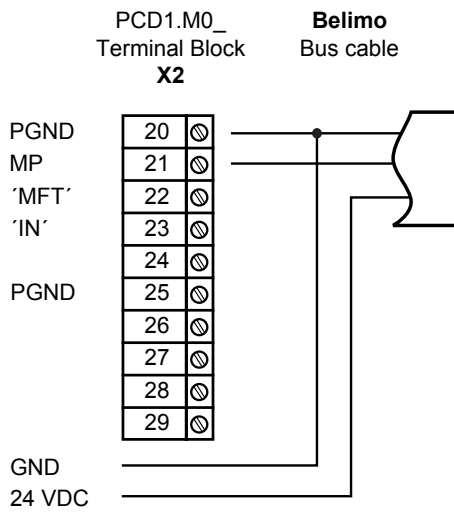
5.2.4 PCD7.F180S Serial Interface Module Belimo MP-Bus

Up to 8 actuators and sensors can be connected.

PCD7.F180S



Cabling



Cabling MP-Bus device

20	PGND	Earth connection, MP string
21	MP	Multi Point The MP bus is the Belimo master-slave bus. Up to 8 slaves can be attached to one master device. They are: - MFT(2) flap drives - MFT(2) valve drives - MFT fire protection flap drives - VAV compact controller NMV-D2M
22	"MFT"	MFT programming device (MP bus internal)
23	"IN"	MFT programming device recognition (input 10 kΩ, Z5V1)
25	PGND	Earth connection, MFT programming unit

6 Configuration (Saia PG5[®] Device Configurator / Device Configuration)

6.1 Requirements

The following description assumes that the user is familiar with the Saia PG5[®] software. If this is not the case, we recommend reading the Manual 26-733 “PG5, software requirements, PG5 V 2.1” (or later).

6.2 General Information

This chapter describes how the Saia PG5[®] Device Configurator is used. The Device Configurator defines:

- cyclical media mapping in order to enable a link between peripheral I/O module values and the device resources (e.g. PCD flags and registers).
- direct access to programming instructions, for reading values from and transmitting values to the peripheral input module.

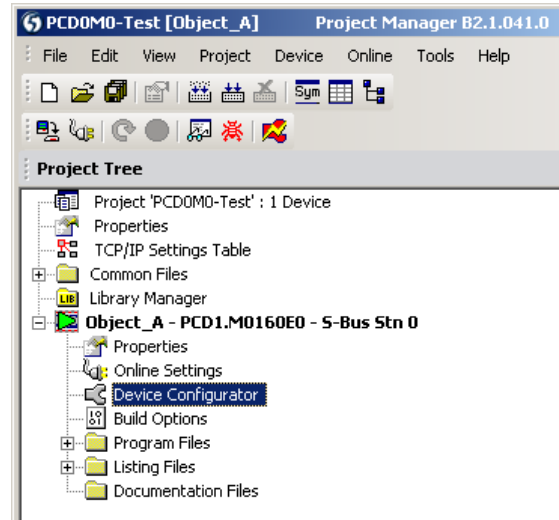


For the PCD1.M0_, I/O handling is always enabled via direct access. There is no “bit” access instruction: the minimum access range is “byte”. You are therefore advised to use media mapping to read and write all I/O channels. For further details, see the online help of the Device Configurator

6.3 Running the Device Configurator

Um HW-Konfiguration, Protokolleinrichtung und E/A-Behandlung einzurichten ist der Device- bzw. Gerätekonfigurator zu verwenden.

The Device Configurator is started by double-clicking on the "Device Configurator" symbol in the project directory tree.

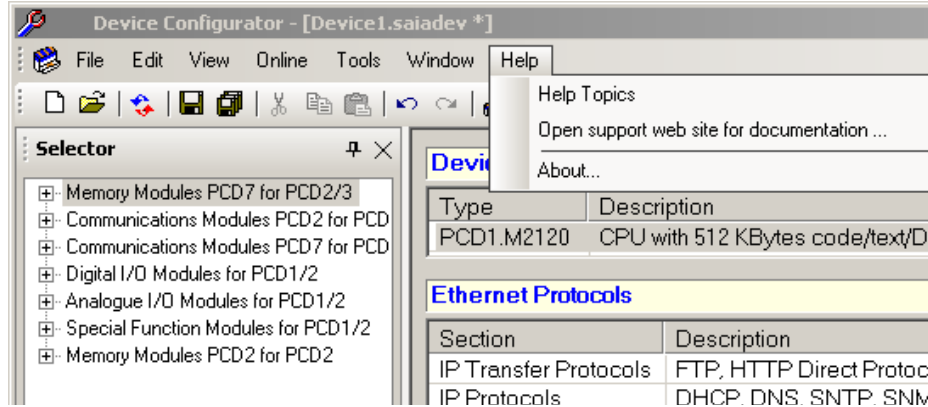


Device		
Type	Description	
PCD1.M0160E0	CPU with 1 MBytes code/text/DB flash memory and 1 MBytes extension memory (RAM für Text/DB from address 4000), 8/6 digital in-/out	
Memory Slots		
Slot	Type	Description
M1		
Monitoring		
Section	Description	
Monitoring	Monitoring and logging of meter data. Automatical scanning of S-Bus meters and gateways.	
Onboard Communications		
Location	Type	Description
Onboard	RS-485/S-Net	RS-485 port for Profi-S-Bus or general-purpose communications.
Onboard	USB	Universal Serial Bus port, PGU or general-purpose.
Onboard	Ethernet	Ethernet port. IP Settings, DHCP.
Socket A		
Ethernet Protocols		
Section	Description	
IP Transfer Protocols	FTP, HTTP Direct Protocols, ODM.	
IP Protocols	DNS, SNMP, SNMP protocols.	
HTTP Portal	HTTP Portal Communication For PCD Over Private Network.	
Onboard Inputs/Outputs		
I/O	Type	Description
I/O 0	16 Digital In-/Outputs	4 digital inputs, 4 digital outputs, 4 configurable in- or outputs, 2 interrupts, 1 PWM, 1 watchdog, connector X0, X1 and X3.
I/O 1	2 Analogue Inputs	2 analogue inputs, -10...+10VDC, 0...20mA, Pt/Ni 1000 or resistance, connector X1.

Properties	
Device: PCD1.M0160E0	
Firmware	
Version	From 1.19.00 or more recent and c
Memory	
User Code/Text/DB Memory	1 MBytes ROM
Extension Text/DB Memory	1 MBytes RAM
User Code/Text/DB Memory I	On File System
User File System Size (Flash)	128 MBytes
Program Directory	Onboard Flash
Options	
Reset Output Enable	No
Time Zone Code	
Password	
Password Enabled	No
Password	
Inactivity Timeout [minutes]	1
S-Bus	
S-Bus Support	Yes
S-Bus Station Number	0
Input/Output Handling	
Input/Output Handling Enable	Yes
Peripheral Addresses Definitio	Auto (recommended)
Power Supply	
Current Available 5V [mA]	500
Current Available V+ [mA]	200
Current Used 5V [mA]	0
Current Used V+ [mA]	0
Web Server	
Default Page	start.htm
Display Root Content Enable	Yes
+ Advanced Parameters	Hide
Web Server Resources	
Time Task Limitation	5
RAM Disk Size	48
Web Server over S-Bus	
S-Bus Web Enabled	Yes
Number Session	8
+ Advanced Parameters	Hide

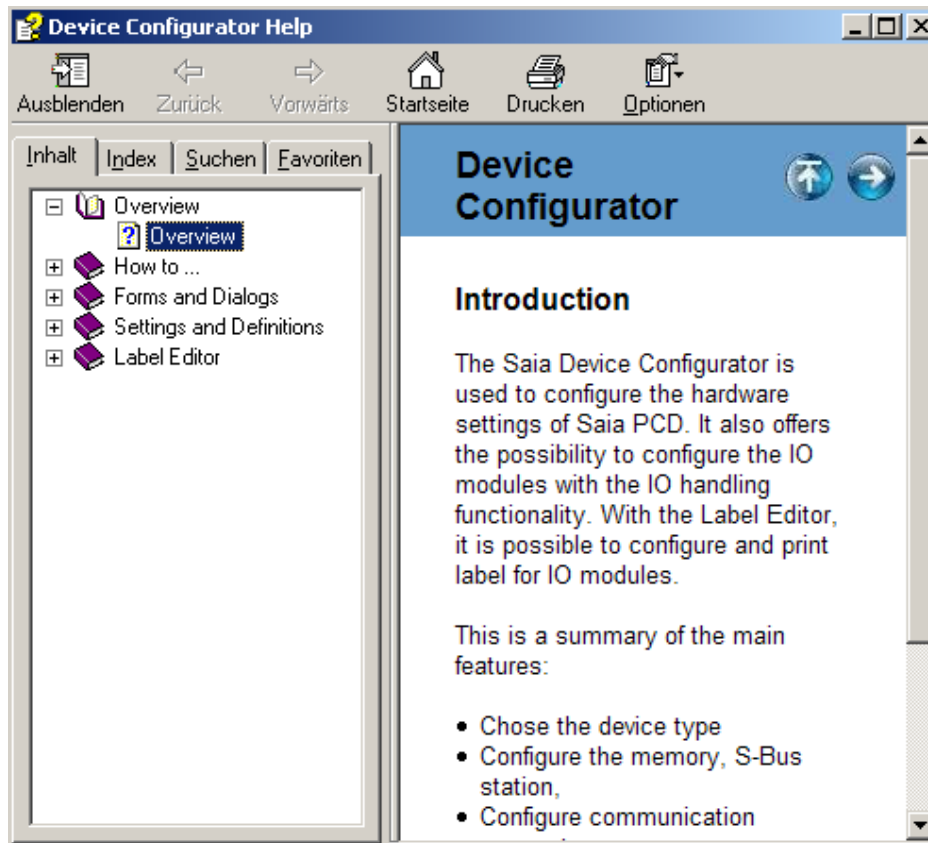
Help

Help for the Device Configurator can be found under “Help Topics” in the “Help” menu:



6

Click on one of the “Help topics”:



6.4 Media Mapping for Digital Inputs on-board

The media mapping of digital inputs uses 16 flags

Media Mapping Digital Inputs	
Media Mapping Enabled For Digital Inputs	Yes
Media Type For Digital Inputs	Flag
Number Of Media For Digital Inputs	16
Media Address for Digital Inputs	16
Flag Symbols Definition for Digital Inputs	(Default)

Mapping table for digital inputs

Symbol Name	Type	Address/Value	Comment	Tags	Scope
ROOT					
IO.Onboard.Digit...	F	16	Digital input 0	S_IO	Public
IO.Onboard.Digit...	F	17	Digital input 1	S_IO	Public
IO.Onboard.Digit...	F	18	Digital input 2	S_IO	Public
IO.Onboard.Digit...	F	19	Digital input 3	S_IO	Public
IO.Onboard.Digit...	F	20	Digital input 4 (usage depends on configuration)	S_IO	Public
IO.Onboard.Digit...	F	21	Digital input 5 (usage depends on configuration)	S_IO	Public
IO.Onboard.Digit...	F	22	Digital input 6 (usage depends on configuration)	S_IO	Public
IO.Onboard.Digit...	F	23	Digital input 7 (usage depends on configuration)	S_IO	Public
IO.Onboard.Statu...	F	24	Status of interrupt input 0	S_IO	Public
IO.Onboard.Statu...	F	25	Status of interrupt input 1	S_IO	Public
IO.Onboard.Statu...	F	26	Status 2 (not used)	S_IO	Public
IO.Onboard.Statu...	F	27	Status 3 (not used)	S_IO	Public
IO.Onboard.Statu...	F	28	Status 4 (not used)	S_IO	Public
IO.Onboard.Statu...	F	29	Status 5 (not used)	S_IO	Public
IO.Onboard.PwM...	F	30	Status of PWM output	S_IO	Public
IO.Onboard.Watc...	F	31	Status of watchdog output	S_IO	Public



6.5 Media Mapping for Digital Outputs on-board

The media mapping of digital outputs uses 16 flags

Media Mapping Digital Outputs	
Media Mapping Digital Outputs Enabled	Yes
Media Type Digital Outputs	Flag
Number Of Media For Digital Outputs	16
Media Address for Digital Outputs	0
Flag Symbols Definition for Digital Outputs	(Default)

Mapping table for digital outputs

Symbol Name	Type	Address/Value	Comment	Tags	Scope
ROOT					
IO.DigitalOutput0	F	0	Digital output 0	S_IO	Public
IO.DigitalOutput1	F	1	Digital output 1	S_IO	Public
IO.DigitalOutput2	F	2	Digital output 2	S_IO	Public
IO.DigitalOutput3	F	3	Digital output 3	S_IO	Public
IO.DigitalOutput4	F	4	Digital output 4 (usage depends on configuration)	S_IO	Public
IO.DigitalOutput5	F	5	Digital output 5 (usage depends on configuration)	S_IO	Public
IO.DigitalOutput6	F	6	Digital output 6 (usage depends on configuration)	S_IO	Public
IO.DigitalOutput7	F	7	Digital output 7 (usage depends on configuration)	S_IO	Public
IO.PwMDigitalOu...	F	8	PWM digital output (usage depends on configurat...	S_IO	Public
IO.RelayOutput	F	9	Relay output (watchdog - usage depends on conf...	S_IO	Public
IO.DigitalOutput10	F	10	Digital output 10 (not used)	S_IO	Public
IO.DigitalOutput11	F	11	Digital output 11 (not used)	S_IO	Public
IO.DigitalOutput12	F	12	Digital output 12 (not used)	S_IO	Public
IO.DigitalOutput13	F	13	Digital output 13 (not used)	S_IO	Public
IO.DigitalOutput14	F	14	Digital output 14 (not used)	S_IO	Public
IO.DigitalOutput15	F	15	Digital output 15 (not used)	S_IO	Public

6.6 Special Functions

PG5 Device Configurator for PCD1.M0160_

Onboard Inputs/Outputs		
I/O	Type	Description
I/O 0	16 Digital In-/Outputs	4 digital inputs, 4 digital outputs, 4 configurable in- or output
I/O 1	2 Analogue Inputs	2 analogue inputs, -10..+10VDC, 0..20mA, Pt/Ni 1000 or res

Properties ▼ ⌕ ✕

I/O 0 : 16 Digital In-/Outputs

- ▶ Media Mapping Digital Inputs
- ▶ Media Mapping Digital Outputs
- ▶ Channels Direction
- ▶ PWM
- ▶ Watchdog
- ▶ Interrupts

6

Select whether channel 4 to 7 should be used as a digital input or output

Select whether the PWM channel should be used as a PWM output or standard output

Select whether the watchdog channel should be used as a watchdog output or standard relay output

Select whether the interrupt channels should be used as interrupts or standard digital inputs

Channels Direction

Direction I/O 4	Input
Direction I/O 5	Input
Direction I/O 6	Input
Direction I/O 7	Input

PWM

PWM Output Usage	Digital Output
------------------	-----------------------

Watchdog

Watchdog Relay Usage	Watchdog
Watchdog Time	250 ms

Interrupts

Interrupt IX0	On rising edge
XOB Number For Interrupt IX0	20
XOB Start Info For Interrupt IX0	0
Interrupt IX1	On rising edge
XOB Number For Interrupt IX1	21
XOB Start Info For Interrupt IX1	0

6.7 Analogue inputs

Onboard Inputs/Outputs		
I/O	Type	Description
I/O 0	16 Digital In-/Outputs	4 digital inputs, 4 digital outputs, 4 configurable in- or outputs, 2
I/O 1	2 Analogue Inputs	2 analogue inputs, -10..+10VDC, 0..20mA, Pt/Ni 1000 or resista

Properties

Mapping setup for values and status or diagnosis

Channel setup and scaling information

I/O 1 : 2 Analogue Inputs	
Media Mapping Analogue Inputs	
Media Mapping For Inputs Enab	Yes
Media Type For Inputs	Register
Number Of Media For Inputs	4
Media Address For Inputs	0
Symbol Definitions For Inputs	(Default)
Media Mapping Status/Diagnostic	
Media Type For Status/Diagnos	Flag
Number Of Media For Status/Di	16
Media Address For Status/Diagr	32
Registers Definition For Status/I	(Default)
Flags Definition For Status/Diag	(Default)
Analogue Input 0	
Filter Analogue Input 0	Off
Input 0 Range	Voltage Input (-10..+10V)
Minimum Value Input 0	-10000
Maximum Value Input 0	10000
Analogue Input 1	
Filter Analogue Input 1	Off
Input 1 Range	Voltage Input (-10..+10V)
Minimum Value Input 1	-10000
Maximum Value Input 1	10000

Mapping table for analogue inputs

Symbol Name	Type	Address/Value	Comment	Tags	Scope
ROOT					
IO.AnalogueInput0	R	0	Analogue input 0	S_IO	Public
IO.AnalogueInput1	R	1	Analogue input 1	S_IO	Public
IO.AnalogueInput2	R	2	Analogue input 2	S_IO	Public
IO.AnalogueInput3	R	3	Analogue input 3	S_IO	Public

Mapping table for status of analogue inputs

Symbol Name	Type	Address/Value	Comment	Tags	Scope
ROOT					
IO.AnalogueInput...	F	32	Analogue input 0 status error	S_IO	Public
IO.AnalogueInput...	F	33	Analogue input 0 status under run	S_IO	Public
IO.AnalogueInput...	F	34	Analogue input 0 status over run	S_IO	Public
IO.AnalogueInput...	F	35	Analogue input 0 status 3 (not used)	S_IO	Public
IO.AnalogueInput...	F	36	Analogue input 0 status 4 (not used)	S_IO	Public
IO.AnalogueInput...	F	37	Analogue input 0 status 5 (not used)	S_IO	Public
IO.AnalogueInput...	F	38	Analogue input 0 status 6 (not used)	S_IO	Public
IO.AnalogueInput...	F	39	Analogue input 0 status 7 (not used)	S_IO	Public
IO.AnalogueInput...	F	40	Analogue input 1 status error	S_IO	Public
IO.AnalogueInput...	F	41	Analogue input 1 status under run	S_IO	Public
IO.AnalogueInput...	F	42	Analogue input 1 status over run	S_IO	Public
IO.AnalogueInput...	F	43	Analogue input 1 status 3 (not used)	S_IO	Public
IO.AnalogueInput...	F	44	Analogue input 1 status 4 (not used)	S_IO	Public
IO.AnalogueInput...	F	45	Analogue input 1 status 5 (not used)	S_IO	Public
IO.AnalogueInput...	F	46	Analogue input 1 status 6 (not used)	S_IO	Public
IO.AnalogueInput...	F	47	Analogue input 1 status 7 (not used)	S_IO	Public

7 Maintenance

7.1 General Information




PCD controllers are maintenance-free, apart from some CPUs, where the battery needs to be changed occasionally.

PCD1 CPUs do not contain any parts which can be replaced by the user. If hardware problems occur, please return the components to Saia-Burgess Controls AG.

7.2 Battery Replacement for the PCD1



Resources (registers, flags, timers, counters, character strings/DBs, etc.) are stored in RAM. To prevent this content from being lost during a power failure, and to enable the hardware clock (if present) to carry on running, PCD1 devices are equipped with a back-up battery:

CPU model	Buffer	Buffer time	Image
PCD1.M0_	Renata CR 2032 lithium battery	1-3 years ¹⁾	

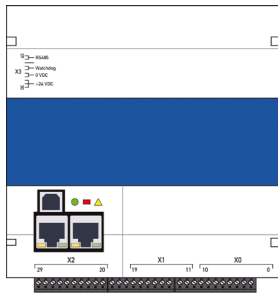
¹⁾ Depending on the ambient temperature: the higher the temperature, the shorter the buffer time

Battery voltage is monitored by the CPU. If the battery is absent or capacity is lost (battery voltage less than 2.4V) the triangular yellow LED blinks and XOB 2 is called.

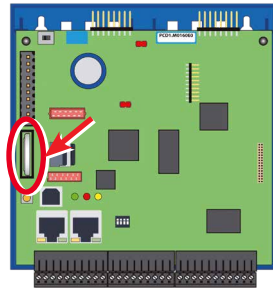


In order to prevent data loss, we recommend changing the batteries while the PCD1 is still connected to the power supply.

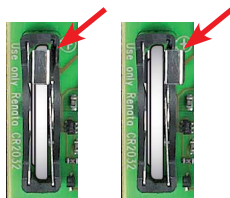
See next page for battery replacement procedure.



Remove the cover of the controller
(see chapter 2.2.5 Removing the Cover)



Locate the battery



Gently press the battery retaining clip to the right



Remove the battery

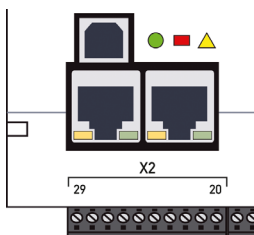


Insert the Renata CR 2032 button battery with the label side (+ pole) up, slightly pushing the battery retaining clip to the side.

The + symbol can also be seen on the circuit board.

-






Fit the housing cover.



Check the battery display (red LED dark)
Battery o.k. = yellow, triangular LED dark
Batteryfailer = yellow, triangular LED blinking

A Annex

A.1 Icons

	<p>In manuals, this symbol refers the reader to further information in this manual or other manuals or technical information documents. As a rule there is no direct link to such documents.</p>
	<p>This symbol warns the reader of the risk to components from electrostatic discharges caused by touch. Recommendation: Before coming into contact with electrical components, you should at least touch the system's negative pole (cabinet or PGU connector). However, it is better to use a grounding wrist strap with its cable permanently attached to the system's negative pole.</p>
	<p>This sign accompanies instructions that must always be followed.</p>
	<p>Explanations beside this sign are valid only for the SBC PCD Classic series.</p>
	<p>Explanations beside this sign are valid only for the SBC PCD xx7 series.</p>



A.2 Definition of Serial Interfaces

A.2.1 RS-232

Designation of signal lines:

Data lines	TXD	Transmit data	[Transmit data]
	RXD	Receive data	[Receive data]
Signal and response circuits	RTS	Request to send	[Transmit part switched on]
	CTS	Clear to send	[Readiness to send]
	DTR	Data terminal ready	[Terminal ready]
	DSR	Data set ready	[Ready for use]
	RI	Ring indicator	[Incoming call]
	DCD	Data carrier detect	[Partner ready]

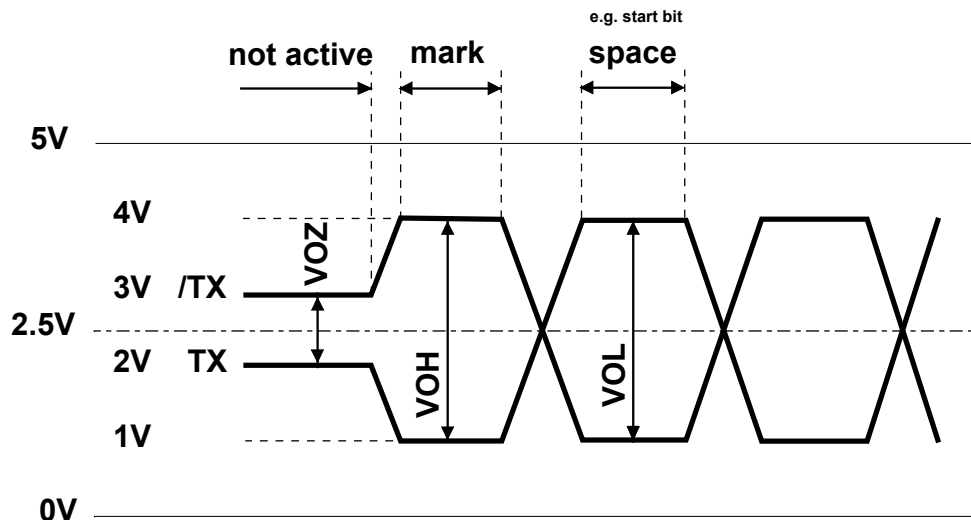
Signals to RS-232

Signal type	Logic status	Setting	Setpoint value
Data signal	0 (empty)	+3 V to +15 V	+7 V
	1 (character)	-15 V to -3 V	-7 V
Control/message signal	0 (off)	-15 V to -3 V	-7 V
	1 (on)	+3 V to +15 V	+7 V



A.2.2 RS-485/422

Signals to RS-485 (RS-422)



VOZ = 0.9 V min ... 1,7 V

VOH = 2 V min (with load) ... 5 V max (without load)

VOL = -2 V ... -5 V

The RS-422 is in idle status in the position “mark”

RS-422:

Signal type	Logic status	Polarity
Data signal	0 (empty) 1(character)	TX positive to /TX/TX positive to TX
Control/message signal	0 (off) 1 (on)	/RTS positive to RTS RTS positive to /RTS

RS-485:

Signal type	Logic status	Polarity
Data signal	0 (empty) 1(character)	RX-TX positive to /RX-/TX/RX-/TX positive to RX-TX



Not all manufacturers use the same connection configuration. Therefore, it may be necessary to cross the data lines.



In order to ensure fault-free operation of an RS-485 network, the network should be closed at both ends. Cables and terminators should be selected according to Manual 26-740 “Installation Components for RS-485 Networks”.

A.3 Glossary

Backup	Datas save on media
Base address	See chapter 2.1.3 “Addressing” → “Plug-in Input and Output Modules”
Compiler	A compiler (from the word compile, to collect) is a program which translates the source text (source code) of another program, which is provided in a specific programming language, into a character sequence that is understandable for the computer.
CPU	Central Processing → Unit Housing with central unit, the heart of the PCD
Device	PLC (Bezeichnung im Saia PG5® Project Manager)
Download	Abb. “DnLD” Save data to PCD
Element	e.g. PLC input, PLC output, flag, register, etc.
Linker	After the compiler has done its work, the linker combines the individual files to create a program.
LIO (Local Input Output)	Inputs/outputs on the CPU (on-board) or connected through the I/O bus (not PCD1) on the CPU.
Media	Media refers to inputs/outputs, flags, registers, etc. in the PCD family.
Media mapping	Assignment of digital and analogue I/O values to flags and registers.
Modules	Carrier cards for input/output electronics
Module holder	CPU, LIO or RIO devices which can accommodate the aforementioned modules.
Motherboard	Main circuit board (CPU)
IL	Instruction list (PCD program code)
NT	New technology, means the PCD generation following the first generation
On-board	means mounted “on the CPU circuit board”
Parsing	A parser is often a type of compiler, which checks the correct syntax of the program.
PGU	Programmable Unit → programming unit
PLC	Process Logic Controller
Port	Interface designation
Buffer battery	Retention of memory content and continuation of the clock after a power supply shut-down.
PWM	Pulse-width modulation (pulse-width modulation is a type of modulation in which a technical measurement (e.g. electric current) switches between two values).
Restore	Saved datas load from media
Resources	In this case inputs or outputs,
RIO (Remote Input Output)	Inputs/outputs on the CPU (on-board) or connected through the I/O bus on the CPU.
Slot	Slot for plug-in
SPM	Saia PCD® Project Manager, main program of the Saia PG5® package

SuperCap	Electronic component (capacitor), which can deliver current for a short time. Retention of memory content and continuation of the clock after a power supply shut-down.
terminated	Reflections at the line ends are prevented through line termination.
PCD2.M2xxx	x in the product designation stands for a number 0..9. In this case it is a three-digit number, such as PCD2.M2110.

A.4 Contact

Saia-Burgess Controls AG

Bahnhofstrasse 18
3280 Murten, Switzerland

Phone central..... +41 26 580 30 00

Phone SBC Support..... +41 26 580 31 00

Fax..... +41 26 580 34 99

Email support: support@saia-pcd.com

Supportsite: www.sbc-support.com

SBC site: www.saia-pcd.com

International Representatives &

SBC Sales Companies: www.saia-pcd.com/contact

A

Postal address for returns from customers of the Swiss Sales office

Saia-Burgess Controls AG

Service Après-Vente
Bahnhofstrasse 18
3280 Murten, Switzerland