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PCD6.M1/2 Summary of Firmware versions

The under summary presents a short description of all firmware versions which are set on PCD6.M1/2 at the production (official version and exceptionally some intermediate version $).
Concerning corrected / known bugs:
Only important bugs are listed here. For other bugs, please refer to the file COMSWERR.XLS that contains more information about known bugs…

Version	PROM	Date	Description
V005	512 KB	01/1991	**Major features:** - Exception handling : XOBs priority mechanism (level1,2,3) - The history list in the debugger - BLOCTEC instructions : XOB11, NCOB, CCOB, SCOB - WORD Instructions : Index register instructions (SEI, INI, DEI, RSI, STI, PUT and GET for DBs and Texts) - INTEGER Instructions : SQR, DIV - GRAFTEC extended to 2000 STEPs and TRANSITIONS - Floating point instructions : FLN, FATAN - Communication instructions : new communication modes (MC4 and MM4), mode MD/SD works with flag ranges > 511, mode MD/SD has different timeout, the instruction SCON, SICL, SOCL - Miscellaneous : Semaphore mechanism (instruction LOCK and UNLOCK), the instruction TEST, memory extension (possibility to put a program > 32K) **Known bugs :** - The RSB (Restart Sequential Block) command causes a crash if more than 25 SBs (Sequential Blocks) are used in one program
V006	512 KB	3/1992	**Major modifications** - The SAIA S-BUS, level I - Expanded LAN2 functions **Correction of known bugs :** In principle, all known bugs in the previous official version are corrected, except the following bugs. **Known bugs / bugs found in this version :** - Transfer the RTC doesn't work with the instruction STXM (level I). - The instruction RCOB doesn't work correctly - Serious problem with indexing (SEI) - Problem with the RTC for years which don't have 53 weeks. - The intruction MOV (Digit) doesn't work correctly when the error flag is set.

			- Programming more than 7 PB and FB levels when XOB 10 was not present causes a crash.
<u>V007</u>	512 KB	6/1993	**Major modifications**

Major modifications

- S-BUS level II (Full S-BUS protocol) up to 19200 Baud, with or without modems
- Reduced and full S-BUS protocol for PCD data transfer (level I) up to 38400 Baud
- Memory extension with PCD7.R3 up to 428 KB
- Special user texts for date and time, registers
- New instructions : TFR (transfer Data), CPBI (Call Program Bloc Indirect)
- The instruction JPI (jump Indirect) has been extended to 8191 program lines

Correction of known bugs :
In principle, all known bugs in the previous official version are corrected, except the following bugs.

Known bugs / bugs found in this version :

- Serious problem with indexing (SEI)
- The communication mode MD/SD is blocked on port 1 when connecting and disconnecting the debugger on PGU port 0.
- Mode C : text output with include texts can cause a crash, only 3 levels of nested texts may be used, the first character in a text should not be "$Lnnnn…"
- It is not possible to download a data block longer than 2048 elements
- The instruction RCOB doesn't work correctly
- S-BUS mode break (SM0/SS0) doesn't work on RS 485 interface
- The indirect text indicators $Rxxxx or @Rxxxx should Always be followed by four digits. If only three digits were Specified in the latest official versions then a crash would occur.
- The STXT instruction transmitted invalid characters if the TEXT specified in the instruction didn't exist. Also, if two ports executed STXT instructions in parallel then the length of the text to be transmitted was occasionally corrupted which caused invalid characters to be transmitted on either of the ports.
- The instructions ALGI/ALGO did not work in the PCD6.
- It was not possible to load a program into CPU 1 when CPU 0 held no program.
- If all the memory extension was assigned to a single CPU and the memory extension security was used then this could cause a timeout on performing a restart cold from the debugger.
- The TEST instruction doesn't work correctly
- If S-BUS PGU is configured to a port which doesn't exist, then all communications are lost and it is no longer

			possible to come online with the PG3
V008	512 KB	1/1994	**Major modifications** - The memory extension did not keep the DB structure in the RAM on battery loss. This has been corrected in the mini project 'memory extension security'. - The S-BUS slave drivers have been modified to make them more tolerant to errors generated by NON-SAIA masters and errors caused by noise on the lines. These modifications have been made in the light of QS problems with S-BUS in several countries whereby a system crash occurs approximately once a week. **Correction of known bugs :** In principle, all known bugs in the previous official version are corrected, except the following bugs. **Known bugs / bugs found in this version :** - Accessing a test > 3999 (for example with STXTX) if the memory extension is not allocated or not present will cause a crash. - Executing an RSB instruction at a STEP which doesn't exist causes an error. This is not detected by the Assembler. - The TEST instruction doesn't work correctly, it has never worked correctly. - Executing a WTIME instruction from CPU 1 can cause the Real Time Clock to be corrupted. (Frequency of error : 1 - 4 times per 24 hours) - Swerrs 124/125/177 The PID instruction is not working correctly for the following Cases. . Proportional factor < 15 and set point > than actual value, when the calculated result of the PID algorithm would be a multiple of 256 then the controlled output (Yn) is set to 0 for one scan. . Integral factor Fi=0 --> then ZS becomes maximum value then Fi is set > 0 --> integrator does not work. To make integrator work a cold start must be performed. - S-Bus communication can cause a problem for the Following case: For one comm. port S-Bus is assigned or configured for 38.4kBd and a second port is assigned for S-Bus < 38.4kBd (e.g. 9600Bd). If on the second port an SRXM instruction to read 32 Registers is executed then the master will perform retries because of the timeout is too short. The intermediate solution is to double the timeout (2 * default value) in the SASI for the second S-Bus port. - Swerrs 179/202

			If a SASI was performed in the background, for instance, with disconnecting/connecting the PG3 to the PCD, then if any communications instruction was being executed there could be a crash.
			- Swerr 184
			  Certain debugger commands which accessed ST/TR's greater than 999 didn't work.
			- Swerr 190
			  MOV instruction error. The MOV instruction would sometimes cause a crash.
			- Swerr 220
			  The SICL instruction didn't work correctly until a SASI had been made on the port concerned
			- Swerr 231
			  The DEFWPR caused a Halt "invalid opcode" on power up
			- In a multiple CPU system, it was not possible to load a program into the own CPU over the S-BUS port if the CPU number was 1 - 6.
			- All four ports on an M260 are put into RS485 active state at
			  Start up.
			- If the program length was greater than 64 Klines or the text length was greater than 256 Kbytes then there would always be a checksum error when the Write Protect was set or the program was loaded into EPROM.
			- The timers decremented too fast after an assignation at 38.4 Kbd.

<u>V009</u>	512 KB	4/1995	**Major modifications** - Password - Gateway - Modems + - New indirect instructions : STXMI / SRXMI, TFRI - New S-BUS function : SRXM to read the system info of a slave, new XOB 17, 18, 19. - Modifications and corrections to the TEST instruction - File load modifications: This has been implemented under S-BUS only. It is now possible to choose whether to clear the outputs during the download or to make a RUN command directly after the download. - The start up routine has been completely rewritten so that the LED's now flash in a new sequence. This routine has new features for extra security. **Correction of known bugs :** In principle, all known bugs in the previous official version are corrected, except the following bugs. **Known bugs / bugs found in this version :** - Swerr 10

The TEST 100 instruction doesn't work correctly when using a PCD6.M1/2 before version 'C'.
- Swerr 11
  Spurious interrupts when using more than one processor which could cause a crash.

- Swerrs 12/13/14
  The user program name of CPU 0 was corrupted when using more than one processor and making a restart cold.
- Swerr 15
  The error "CPU SYNCH ERROR" occurred on CPU's 1 to 6 occasionally after a restart cold.
- Swerr 16
  The S-BUS Gateway didn't work correctly on CPU's 1 - 6 if a restart cold 1 - 6 was made.
- Swerr 17
  When using S-Bus PGU, the CPUx does not go in Stop After a Restart Cold/Warm x command if communication is Active on another CPU.
- Swerr 18
  On PCD6.M220/M260 port RS-485 are active after start up
- Swerr 19
  On multi-CPU's system the CPU, occasionally after a Restart cold the CPU's detect an HW error.
- Swerr 21
  On PCD6, Sbus PGU PLM assignation cause trouble on CPUs without a PGU port assignation. On this CPUs the Port 3 does not work properly
- Swerr 126
  SCOB instruction doesn't work correctly.
- Swerr 130
  When in trace in GRAFTEC, if a condition is TRUE in the Transition then the transition is active, but the next step has already been executed.
- Swerr 218
  The error flag problem with the SASI instruction, this includes the whole concept of the error flag.
- Swerr 227
  Problem with password when using F-SBUS Gateway
- Swerr 230
  Problem with MD/SD mode when transmitting the RTC.

- Swerrs 234/235
  The break length definition doesn't work correctly with SM0 mode

The following bugs will not be corrected in the next version because there is not enough place in the FW EROM 512 KB.
- Swerrs 124/125/177/ 279
  Problems with the PID instruction.

			- Swerr 132 When in trace in GRAFTEC, if a condition is TRUE in the Transition then the transition is active, but the next step has Already been executed. - Swerrs 143/187/204/194/212/215/236 SYSRD/SYSWR modifications are not implemented in the PCD6. - Swerr 226 The 'NEW FEATURES FOR THE PG3 DOWNLOADER **/DEBUGGER/CONNECT MENU'** - Swerr 282 JPI instruction to accept values greater than 8191, for Example up to 32 bits. - Swerr 276 Adaptations for XOB 8 (invalid opcode) in multi-CPU Environments. - Swerr 279 The PID instruction : When the Fi factor is zero, the Zs Value was falsely initialised to a large value.
V$9B	512 KB	01/1998	The startup routine has been modified for compatibility with PCD6.M3 CPUs (only Version 001).
V$9C	512 KB	03/1998	The startup routine has been modified for compatibility with PCD6.M3 CPUs (only Version 001).
V00A	512 KB	01/1999	**Only this version is compatible with the firmware version V002 of the PCD6.M3, due to the new RTC management. Older versions are not compatible anymore.** **Major modifications** - The startup routine has been modified for compatibility with PCD6.M3 CPUs. - The "Reserve Int" routine has been corrected and no more "68k Invalid OPC" error happens if this interrupt routine is called. - Instruction SOCL is now possible on port configured as Sbus PGU - New RTC management. That means: . Calculation of WEEK NUMBER and DAY NUMBER is compliant to ISO8601 and Year 2000. . The day number and the week number are irrelevant when loading time values (WTIME, STXM...). **Correction of known bugs :** In principle, all known bugs in the previous official version are corrected, except the following bugs. **Known bugs / bugs found in this version :** - All known bugs listed above (see version 009) cannot be corrected because of not enough places in the FW.

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